# Autonomous readout ASIC with 169dB input dynamic range for amperometric measurement

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***Abstract*—A readout circuit for the measurement of amperometric sensors is presented. The circuit consists of analog frontend (AFE) and an automatic gain adjustment circuit to tune the gain of the AFE according to the input current covering a wide dynamic range of 169dB and a minimum input referred noise of 44 fA. The circuit is implemented in 0.35 $\mu$m technology, consumes 5.83 mW from 3.3 V supply voltage and occupies 0.31 $mm^2$ silicon area.**

***Index Terms*—Amperometric sensing, readout circuit, CMOS, wide dynamic range, automatic gain control**

## I. Introduction

A new generation of *Implantable and Wearable Medical devices* (IWeMed) are emerging to enable continuous monitoring of small biomolecules (e.g. glucose, hormones) in the human body. Such IWeMed technology eliminates the need for blood sampling and, through continuous measurement, addresses unmet clinical needs in predictive diagnostics and self-monitoring and management of health.

An IWeMed has to be small, fully-integrated, and wireless to be minimally invasive. Moreover, it should be able to detect specific group of key metabolites and drugs within a single platform, to accurately monitor the health condition of the patient. Most existing biosensing systems consist of the combination of fluidic systems, sensors and electronic circuits to readout the sensors.

To date, several medical devices use electrochemical sensors. A notable example is the continious glucose measurement devices for diabetes. The electrochemical sensor work based on the principle of electrochemical detection using probe molecules and enzymes to detect the target analyte. The sensor outputs a current to be measured by the instrumentation electronics. In a multi-analyte sensing device, the sensor currents may vary within a wide range (several decades) [1] and even vary from day to day. Therefore, the instrumentation needs to be tuned for each measurement and each sensor.

Autonomy is a key requirement in developing IWeMeds for minimally invasive, low-cost and long-term monitoring of different biomolecules. However, existing devices are not autonomous because, for instance, the readout electronics requires external tuning to be adjusted to different sensors with different signal levels [2]–[4], and the sensors need frequent recalibrations to detect their time-varying sensitivity [5]. These require human intervention, imposes extra costs, and ultimately limits the progress of IWeMed technology.

In this work we present, for the first time, the design of a readout circuit capable of automatic self-adjustment to measure currents within a wide dynamic range. An *automatic gain adjustment* (AGA) algorithm is developed and implemented on-chip to eliminate the need for manual tuning. The design of the system comprising analog and digital parts is presented in the next section, followed by simulation results in Section III.

## II. System design

The readout circuit comprises (i) an *analog frontend* (AFE) capable of measuring currents within a wide dynamic range from 1 pA to 10 $\mu$A to cover a wide range of amperometric sensors. The wide range is achieved through several gain settings by changing tuneable parameters such as integrating capacitor and the integration time; (ii) A gain adjustment block to determine the correct gain and change the related parameters (capacitance, integration time) in AFE based on the input current; (iii) a 10-bit ADC (from standard AMS library cell) which is activated only after the correct gain setting is determined and set by AGA.

The readout circuit switches between two operation modes: readout mode, where ADC is up and running, and *Automatic gain adjustment* (AGA) mode where the gain is being determined. The AGA circuit also outputs the gain settings that can be used together with the digital output of the ADC to interpret the data.

### A. Analogue frontend

A switched-capacitor integrator (SCI) is designed to apply a fixed voltage to the sensor and to measure the sensor current. The SCI architecture is chosen because its parameters can be easily adjusted digitally. The schematic view of the SCI circuit is shown in Fig. 1. It consists of a amplifier, integrating capacitors and switches. A single-stage folded cascode topology is chosen as it provides high gain and ensures stability for a wide range of capacitive load. As shown in Fig. 2, large transistors are used for the input differential pair to achieve high transconductance and minimise flicker noise and mismatch. The dimensions of the transistors are chosen carefully to ensure they operate in the saturation region for a wide range of input currents. The maximum output current of the transconductance amplifier is set close to the maximum input current expected from the sensor (10 $\mu$A).

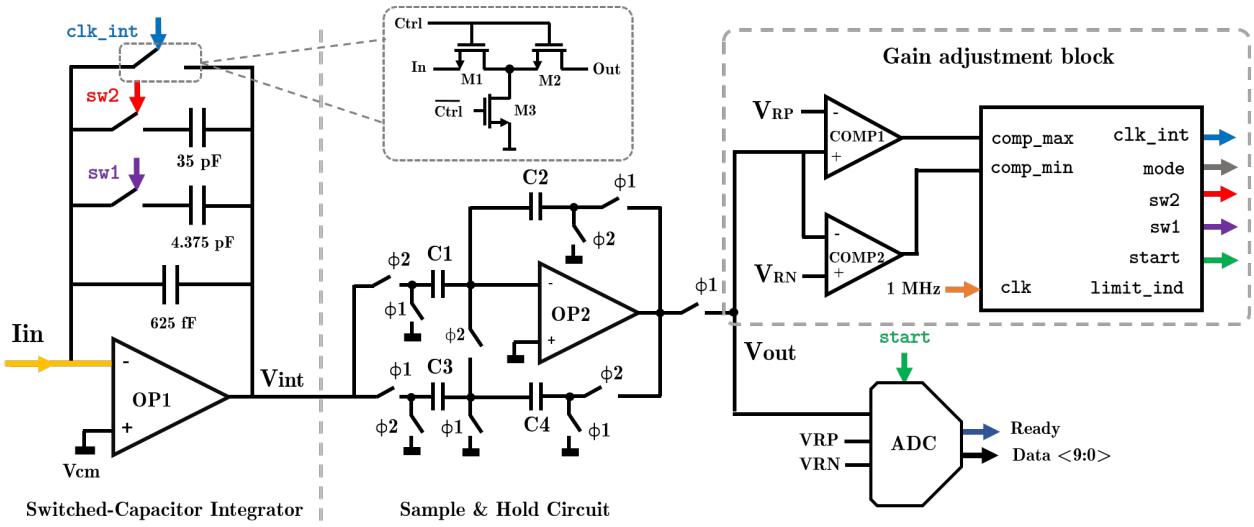


Fig. 1. The block diagram of the proposed readout circuit with autoimatic gain adjustment

A low-leakage switch in parallel to the capacitor controls the reset and integration times. When the switch is open, the sensor current flows through the capacitor and generates an output voltage, $V_{int}$. When the switch is closed, the sensor current flows through the switch and thus the current ensuring there is always a path for the sensor current during both reset and integration phases. The output of the integrator at the end of the integration phase can be calculated by

$$V_{int} = \frac{T_{int} \times I_{in}}{C_{int}} \quad (1)$$

where $T_{int}$ is the integration time, $C_{int}$ is the total feedback capacitance in the TIA, and $I_{in}$ is the input current to the ciruit.

The minimise gain error due to the leakage of the switch, a low-leakage switch structure is implemented. This is based on the floating-body techniques where an extra lateral transistor, M3, reduces the leakage maintains a zero voltage across the M1 and M2 during the integration time.

The output of the switched-capacitor integrator is sampled during the integration phase and held during the reset phase, to be sent either to the ADC or to the AGC circuit. The sample and hold circuit is adopted from [6] and chosen due to its small slew rate demand on the amplifier and its auto-zeroing feature. Here Φ1 and Φ2 are non-overlapping clock phases to drive the switches and correspond to the reset and integration phases, respectively.

### *B. Automatic Gain Adjustment (AGA)*

The whole input current range is divided into eight sub-ranges we refer to as modes. The gain in each mode is set through adjusting the SCI feedback capacitors and/or the integration time. The gain is chosen so that $V_{OUT}$ remains within a certain range $(V_{RN}, V_{RP})$ in order to avoid nonlinearity and ensure 10-bit resolution can be achieved in each sub-range using a 10-bit ADC.

The clock waveform is generated in the AGA system based on an external clock of 1 MHz. The genetrated clock

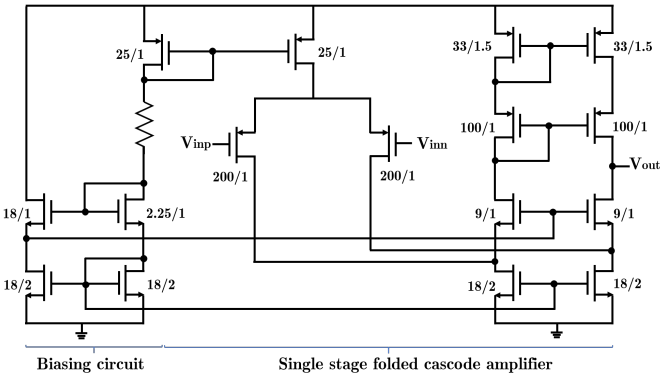


Fig. 2. The schematic of the folded-cascode amplifier used in $OP_1$ and $OP_2$

waveforms provide a fixed reset time (12 $\mu$s) with various integration times (5 $\mu$s, 40 $\mu$s, 320 $\mu$s, 2.56 ms, 20.48 ms, 164 ms)). The AGA circuit also provides the control signals to change the total capacitance to one of 625 fF, 5 pF, 40 pF.

Two comparators compare output of the sample and hold at every clock cycle with an upper ($V_{RP}$) and a lower threshold ($V_{RN}$). Here clock-based comparators are chosen to reduce the total power consumption since the comparator is only needed after integration phase. The schematic of the comparator is shown in Fig. 4. The output of the comparators are used to detect in range or out of range samples. The comparison is repeated during N clock cycles to minimise the effect of instantaneous noise on the results. The AGA decides whether there is a need to change the mode only if the percentage of the out of range samples is higher than a threshold value, for example 50%.

A state diagram for the autonomous gain control algorithm is presented in Fig 3. At the start-up the circuit enters the AGA mode to determin the mode. Here the initial mode is set to the lowest gain to prevent AFE saturation in case the current belongs to the highset sub-range. Once the mode is determined the ready signal is inserted to activate the ADC

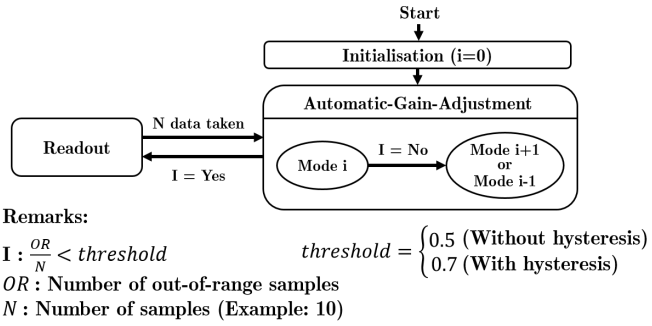


Fig. 3. The state diagram for autonomous gain control.

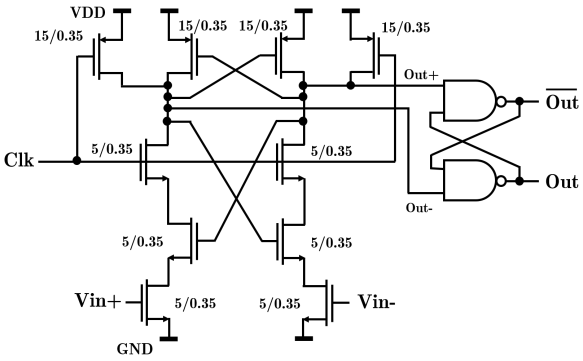


Fig. 4. The schematic of the clocked comparator.

and the cirucit enters the readout mode. The circuit remains in the readout mode for another N clock cycles before going bacl to AGA mode to check/adjust the gain again.

*1) Hysteresis Operation:* To ensure the mode changing during AGA phase does not create mode oscillations, a hysteresis operation is designed and embedded into AGA. The mode oscillation can happen for instance if the input current is in between two modes or if a large electrochemical noise [7] causes multiple crossings between two modes. The hysteresis operation is implemented by altering the out-of-range sample threshold from 50% to 70% everytime the AGA phase is activated after a readout phase. The circuit will therefore tend to stay in the current mode unless the change in input current is large and long enough.

## III. Simulation Results

The circuit is designed in AMS 350nm technology with two poly and four metal layers. The layout is presented in Fig. 5 occupying a total area of 0.31 $mm^2$. The whole circuit consumes 5.83 mW from a 3.3 V supply voltage in the initial mode (highest clock frequency, largest capacitor). The minimum input referred noise of the AFE is 44 fA at highest gain. The maximum input current that can be measured with less than 3% nonlinearity is 13 $\mu$A leading to an overall input dynamic range of 169 dB.

To characterise the system a number of simulations are performed and presented here. Fig. 6 illustrates how the system responds to an input step from 250 nA to 45 nA and reverse (i.e. from mode 1 to mode 2 and reverse). The AGA

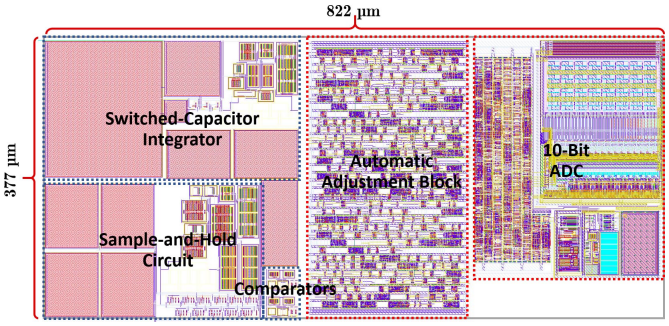


Fig. 5. Complete system layout with annotated floorplan

circuit initially starts from mode 0 and goes to mode 1 to accommodate for 250 nA. After the step change in the current, the mode changes to 2 and gain increases. Then, the circuit enters the readout mode and, after acquiring ten samples, goes back to the AGA mode. Here since the input current has changed significiantly the mode changes again.

Parametric simulations is shown in Fig. 7 demonstrating the mode is detected correctly at the end of the first execution of the AGA phase after start-up. The transient simulation shown in Fig. 8 illustrates how the systems changes the mode dynamically duirng a traingular input current. The delay, $t_{d,ij}$ between when the current crosses between two modes i and j to the time when the AGA circuit updates the mode is calculated by:

$$t_{d,ij} = (N-p)T_{clk,i} + N \times (T_{clk,i+1} + ... + T_{clk,j}) \quad (2)$$

where $T_{clk,m}$ is the period of the clock in mode m, $N$ is the number of samples taken in a single AGA cycle (10 in our design), and $p$ is the number (between 1 and N) of the readout cycle where the current has entered the new sub-range.

A comparison with state-of-the art indicates that out proposed circuit is the first readout circuit that automatically adjusts itself to the input current range (See Table I,). The circuit can measure a variety of sensors without need for manual or external tunning.

## IV. Conclusion

The readout circuit introduced in this report can measure currents within 13 $\mu$A with a minimum input-referred noise of 44 fA. A mixed-signal gain control system adjusts the gain according to the input current levels. Eight different gain values are achieved by changing the integration time and the integrating capacitance values covering a wide input dynamic range of 169 dB. An embedded hysteresis function is designed to ensure stability when input current is in between two modes as well as in presnece of large electrochemical noise.

It is believed that this circuit has advanced the basis of autonomous biosignal analysis, which pushes the boundary of the development of IWeMed technology.

## V. Acknowledgement

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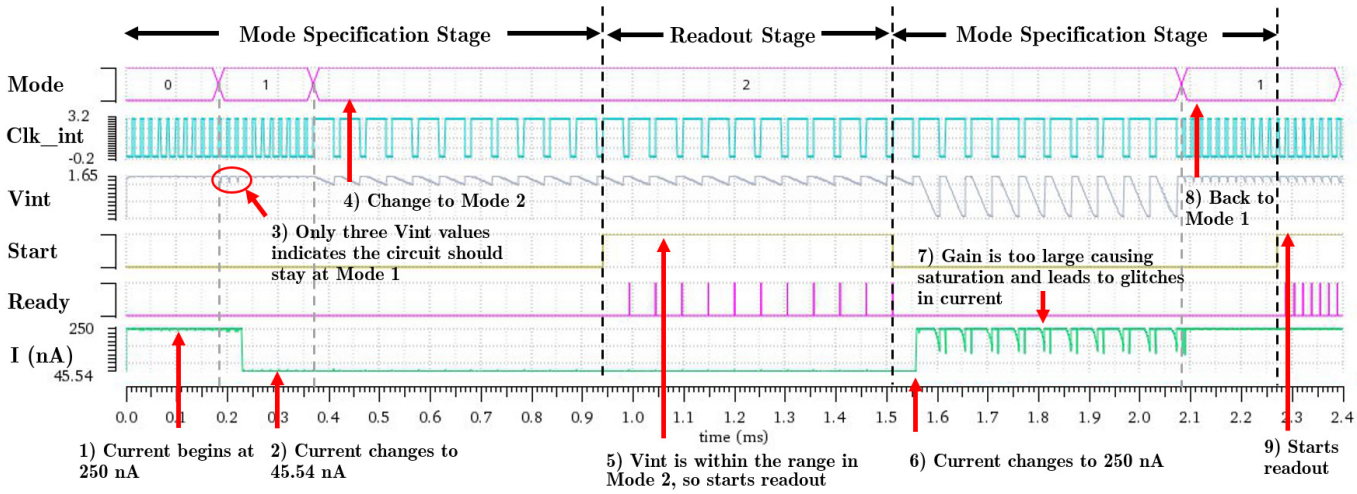


Fig. 6. Readout circuit operation for a step change in the input current. The circuit transitions to a suitable mode based on the input current and performs ADC conversion during readout stage. (Follow steps 1 to 9)

TABLE I
COMPARISON WITH THE STATE-OF-THE-ART

| Paper | Technology ($\mu$m) | Min current (pA) | Max current ($\mu$A) | Dynamic range (dB) | Power (mW) | Gain settings | Autonomous adjustments? |
|---|---|---|---|---|---|---|---|
| TBCAS'13 [2] | 0.35 | 24 | 0.35 | 83 | 0.19 | 2 | No |
| TBCAS'07 [3] | 0.5 | 0.1 | $\pm$0.5 | 134 | 1.27 | 9 | No |
| TBCAS'16 [4] | 0.5 | 0.1 | 16 | 164 | 0.241 | 4 | No |
| TBCAS'17 [8] | 0.35 | 0.47 | $\pm$20 | 153 | 9.3 | 4 | No |
| TBCAS'18 [9] | 0.5 | 7.2 | 0.11 | 84 | 0.021 | 2 | No |
| **This work (simulated)** | **0.35** | **0.044** | **$\pm$13** | **169** | **5.83** | 8 | **Yes** |

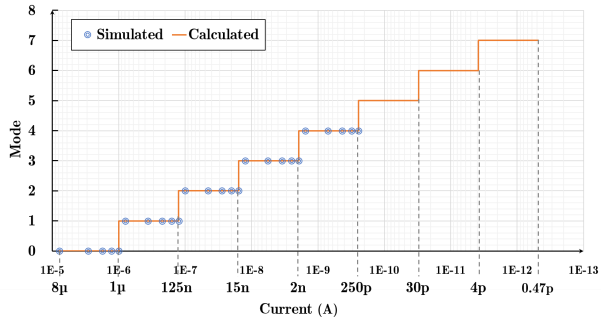


Fig. 7. Simulated characteristics of the whole system showing the final mode determined by AGA circuit vs the input current

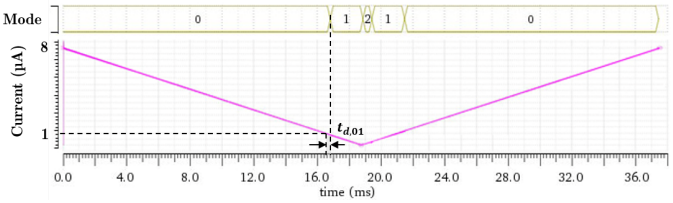


Fig. 8. Mode changes with respect to input current

design. S. Ghoreishizadeh acknowledges the support of the Imperial College Junior Research Fellowship scheme.

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