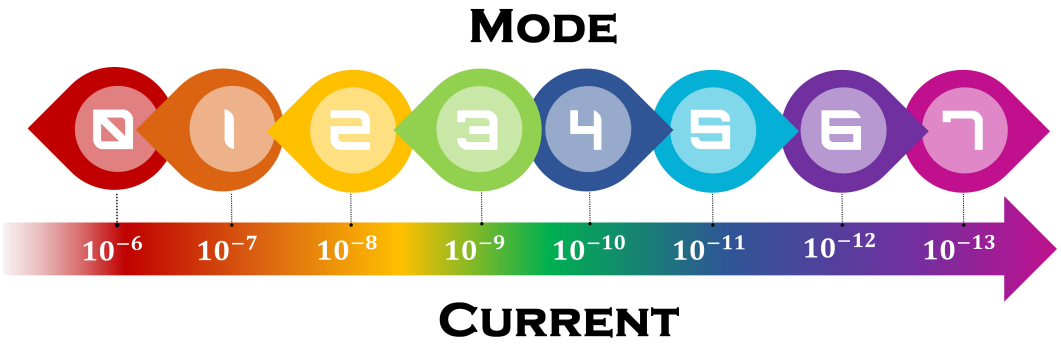
Imperial College London

Department of Electrical and Electronic Engineering

Final Year Project Report 2018



Project Title:	**An Autonomous Readout Circuit for Amperometric Bio-sensing**
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Abstract

In this modern world, most of the medical devices are equipped with biosensors. For example, a biosensor which is based on the electrochemical detection principle is capable of measuring different metabolites such as glucose and lactate in a single finger-stick blood sample. This is achieved by capturing the concentration of the analytes and translating them into an electronic information domain.

This report describes the principle, design process and simulation of an autonomous gain control readout circuit which is capable of measuring current from the working electrode of a sensor with wide dynamic range. The whole system is implemented and simulated using Cadence Hit-Kit v4.10. A mixed-signal integrated circuit is implemented using cadence 350 nm technology. Its analogue part is presented in the report to demonstrate its performance in terms of sensitivity, linearity, dynamic range and noise. The range of the input current of the system is $\pm$ 13 μA with minimum input-referred noise of 44 fA from 3.3 V supply.

To date, there are different topologies of the state-of-the art readout circuits for amperometry biosensors. However, an autonomous gain control readout circuit is introduced and demonstrated for the first time in this report. It enables the system to autonomously vary its operation mode successfully to measure the sensor current. The autonomous gain control algorithm is implemented using Hardware Descriptive Language.

Acknowledgements

This report would not have been possible without the contributions of a few key individuals. First and foremost, I would like to express special gratitude to my project supervisor, Dr. Sara Ghoreishizadeh, who in spite of her extraordinarily busy schedule, invested her full effort in guiding me to achieve my project goal. I wish to thank her for her patience and constant guidance and encouragement in the past 9 months. I have been fortunate to learn so much from her technical insight and mentorship.

My thanks and appreciations also go to my co-supervisor, Dr. Pantelis Georgiou who equipped me with invaluable knowledges through all his lectures such as Analogue Integrated Circuit and Systems, Analogue Signal Processing and Biomedical Electronics courses. I wish to thank him for inspiring me to undertake this bio-inspired technology project which I enjoyed throughout the duration of the project.

Furthermore, I would also like to acknowledge the crucial roles played by the research staffs and postgraduate students of Imperial College Centre for Bio-Inspired Technology. Special thanks to Michal, Lieuwe and Nicolas for providing me with technical support on Cadence. I wish to thank Song Luan for giving me vital suggestions and feedback on the digital part of my circuit.

I would also like to thank my friends who supported and encouraged me to strive towards my goals. Many thanks goes to Usama for helping me to debug my VHDL code; Esther for proof-reading my report and giving me suggestions to make my report more presentable.

Last but not least, I would like to express my appreciation to my beloved family. Their words of encouragement and support have strive me towards the completion of my final year project.

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Nowadays, as health care systems are increasingly stressed, patients are being discharged from hospitals and other healthcare institutions still needing extra care and attention. Patients with chronic illness such as hypertension, diabetes or kidney failure need to constantly monitor their body conditions. Hence, both patients and professional caregivers utilise a wide variety of biosensors in non-institutional settings to manage their own health, assist others with healthcare, and receive assistance with health management [1]. This leads to an increase in demand and development in biosensors where its market is expected to reach approximately USD 360 million by the end of 2023 [2]. These technologies provide support not only for care related to acute and chronic medical conditions, but also for disease prevention and lifestyle choices.

Non-clinical handheld devices to measure different metabolites (such as glucose and lactate) in a single finger-stick blood sample have been developed based on the principle of electrochemical detection using enzymes. Each sensor generates a current which indicates the concentration of targeted metabolite. However, they need to be tuned for each measurement and sensor. Consequently, autonomous gain is needed to be rendered with these technologies while making sure the biosensors are safe, reliable, and effective for use in non-clinical environments. Hence, users of wider demographic can use the biosensors and benefit from these technologies.

1.1 Project Specifications

The project involves the creation, implementation and test of a current readout circuit to measure sensor current within a wide range of 1pA to 1μA. An automatic-gain-adjustment algorithm should be developed and implemented on-chip to eliminate the need for manual tuning of the front-end electronics.

1.2 Challenges

The main challenges of the project are listed below:

1. Familiarisation and mastery in Cadence tools.
2. Implementation of a readout circuit capable of measuring a wide dynamic range of input sensor current by sectioning into different operating modes.
3. The linearity of the decimated output corresponds to the input current in each operating mode.
4. Implementation of a digital circuit to perform autonomous gain control by using Hardware Descriptive Language (VHDL).
5. Implementation of hysteresis operation in the digital circuit to avoid oscillation between modes.
6. The timing of the integrator, comparator, sample and hold, and ADC of the system.
7. Implementation of suitable simulations or testbenches to model the performance of the system.
8. Optimisation of the system in terms of power consumption, noise and area.

1.3 Report Outline

Following an introduction, this report is organised as follows:

Chapter 2 describes the literature survey of the project. The basic electrochemical detection principle is explained. Different state-of-art readout circuits which are capable of achieving a wide dynamic range of current are studied. A comparison is then made to compare their performances.

Chapter 3 focuses on the implementation plan of the project. It describes the initial architecture of the proposed circuit and its simulation results. However, the performance of the initial architecture is below expectation. This leads to the implementation of a different topology which will be discussed in following chapter.

Chapter 4 describes the analogue part of the circuits in which the design choices are justified, followed by an overall block diagram and the simulation result in terms of dynamic range and noise.

Chapter 5 focuses on the digital part of the circuit. The autonomous gain algorithm is explained and implemented in VHDL. The RTL simulation result of the algorithm in ModelSim is presented as well.

Chapter 6 presents the system level simulation of the readout circuit to demonstrate its performance. Transient simulations with noisy signal and varying current are presented. Parametric simulation

which shows changes in mode across input current is also presented.

Chapter 7 describes the layout of the readout circuit. Different layout techniques are discussed and present in this chapter, followed by the logic synthesis flow of the digital circuit. The layout is then presented at the end of the chapter.

Chapter 8 contains a conclusion where a summary of the achievements that have been accomplished is presented. The future works are also discussed to point out possible modifications and improvements that can be made to improve the performance of the system.

Chapter 2

Biosensors - State of Art

2.1 Electrochemical Detection

Among the technologies for bio-sensing [3], electrochemical detection techniques have been extensively researched and developed to capture biorecognition events and translate the results into electrical signals. Electrochemical biosensors have several advantages in terms of their performance and utility. For example, they allow label-free detection which reduce time, cost and complexity compared with the use of sample labeling techniques. They also allow continuous real-time measurement in which the concentration of a target metabolite can be determined from time to time. They are well-suited for miniaturisation as well. The electrochemical detection principles such as sensing and readout are explained in detail in the following subsections.

2.2 Sensing Circuit

The three-electrode system is one of the most popular topologies for translating biorecogntion responses into electrical signals. This can be achieved by immobilising biorecognition elements which are capable of selectively recognising the target analyte on the working electrode (WE) where biochemical processes take place. The reference electrode (RE) supplies a stable reference voltage to the analyte without any current flow on it. The counter electrode (CE) completes the circuit by suppling the sensing current which flows in the WE. The three-electrode system is able to eliminate the undesired IR drop error [4] in the two-electrode system which only consists of the WE and RE.

2.3 Readout Circuits

The readout circuits are essential to amplify and process the sensor current from the working electrode and provide front-end signal conditioning. The sensor current is typically within a wide range and varies from time to time depending on the target analyte. Hence a well-designed readout circuit must be able to amplify or process the small sensor current accurately while keeping the signal-to-noise ratio

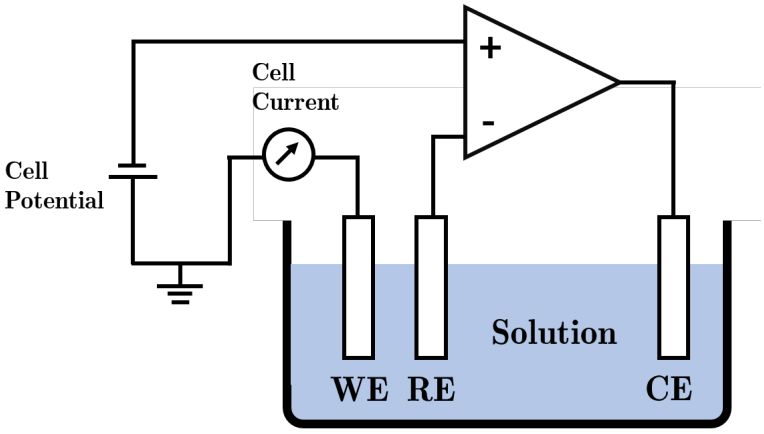


Figure 2.1 Three electrode system

low. Different readout circuits for a wide dynamic input current range are discussed and evaluated in the following subsections and a comparison between the circuit structures is tabulated thereafter.

2.3.1 Current-to-Time Conversion Circuit

Time-based converter [5] as shown in Fig. 2.2 is one of the most popular readout circuits in which the readout current is converted into time. Time-based conversion can be achieved by measuring the time to discharge a pre-charged capacitor (C_d). The capacitor is discharged through the transistor N1 with the input current flowing through WE. The relationship between time to discharge and input current is given by the equation 2.1.

$$\Delta t = \frac{C\Delta V}{I_{in}} \tag{2.1}$$

2.3.2 Current-to-Frequency Conversion Circuit

The sensor current can be converted into frequency using an I-to-F converter. Fig. 2.3 depicts an example of an I-to-F converter [6]. The input current from the WE is mirrored to minimise the kickback effect of the I-to-F converter to the potentiostat. The mirrored current is then integrated at the capacitor. The D-flip flop generates an output pulse which is proportional to the input current by setting or reseting the pulse based on the difference between voltage at the capacitor and two threshold voltages. Hence the output frequency is generated.

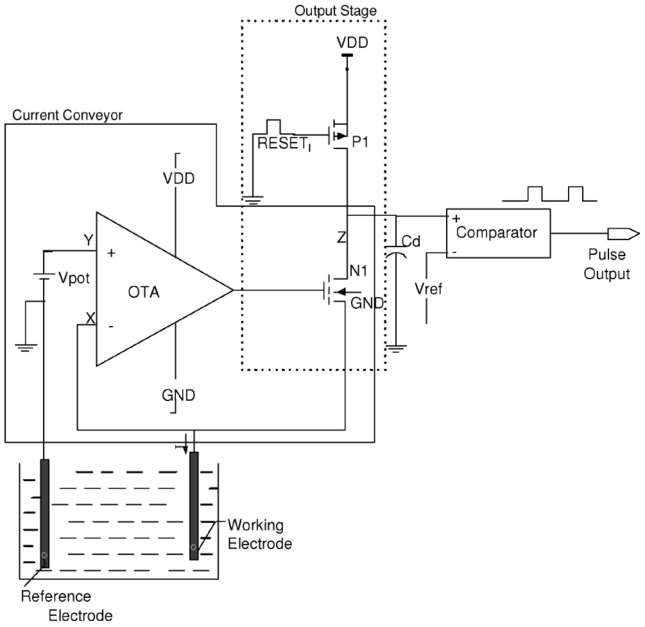


Figure 2.2 VLSI potentiostat using a NMOS transistor at the input, used to discharge the capacitor to convert input current into time. Reprinted from [5].

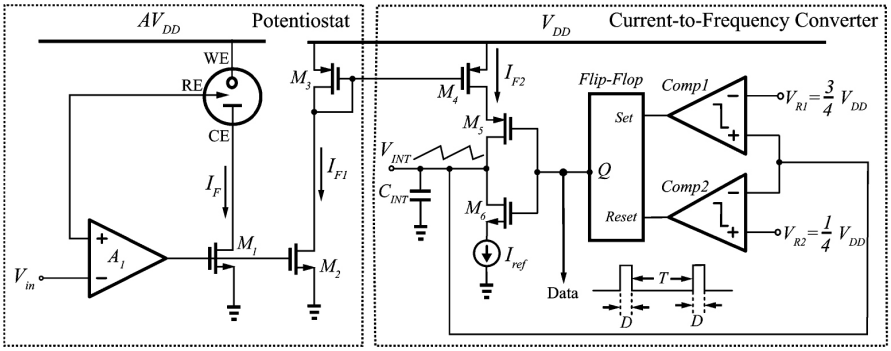


Figure 2.3 Simplified schematic of the potentiostat and I-to-F converter. Reprinted from [6].

2.3.3 ΣΔ based Circuit

Sigma delta (ΣΔ) based circuits digitize the input current through ΣΔ ADC.

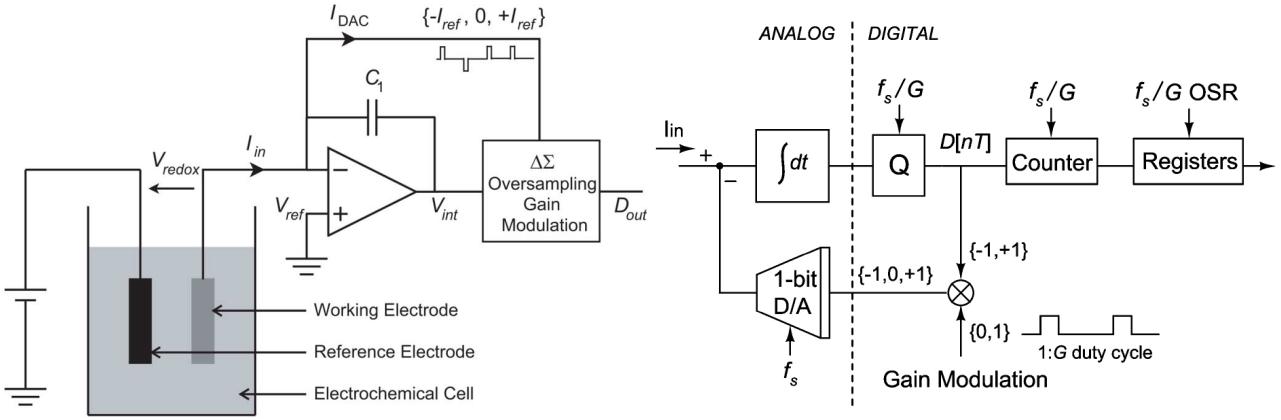
Feedback-modulated ΣΔ

The ΣΔ modulator which consists of a current integrator, comparator and single-bit DAC is implemented at the feedback loop as shown in Fig. 2.4 [7]. The wide dynamic range of input current which spans over 6 decades is achieved by tuning the delta-sigma oversampling ratio (OSR) and digital gain (G) of the gain-modulation scheme. In the gain-modulation scheme, the duty cycle (1/G) of the shunting sequence in the D/A feedback loop of the ΣΔ modulator varies based on the input current and sets the gain of the input amplification. Since the duty cycle effectively shunts the strength of the reference current in the D/A feedback loop by the same factor, this gives the relationship between input current

and reference current as shown in equation 2.2, where the first term represents the decimated output, and the second term represents the conversion error.

$$I_{in} = \sum_{i=1}^{OSC-1} D[i] \frac{I_{ref}}{G\,OSR} + \frac{V_{int}[OSR]}{OSR} \frac{C_1}{T} \tag{2.2}$$

The digital gain modulation over G clock cycles increase the conversion time by a factor of G. As seen in the equation, the OSC can be increased instead of G. However, increasing G is preferred since it produces more precise results owing to reduced noise.



(a) Simplified schematic of the potentiostat system

(b) System level diagram

Figure 2.4 Feedback-modulated ΣΔ based circuit. Reprinted from [7].

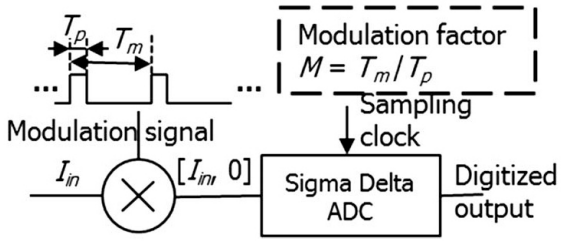
Input-modulated ΣΔ

Another example of ΣΔ based circuit is the input-modulated ΣΔ [8]. The circuit concept is similar to that of the feedback modulated ΣΔ, but the digital modulation happens at the input stage before the ΣΔ ADC stage. The input current is modulated wih a square wave with duty cycle of 1/M. This reduces the requirement for ΣΔ ADC reference current by a factor of M since the average current seen by the ADC input is reduced by a factor of M as well.

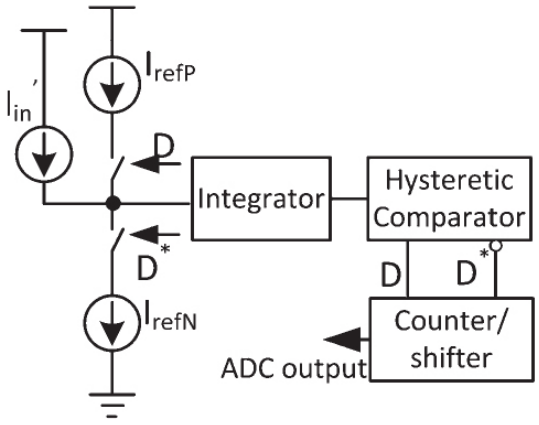
The ADC comprises a current integrator and a hysteretic comparator to produce two bit 1-bit pulse-width-modulation (PWM) digital pulses, D and D*. The digital pulses are used to modulate two reference currents, I_{refP} and I_{refN}.

2.3.4 Voltage-mode Circuit

The use of voltage-mode circuit is the simplest approach to measure the sensor current by translating the input current to voltage directly through a resistor, capacitor or switched-capacitor integrator. It is the most common approach for redox current acquisition [9, 10].

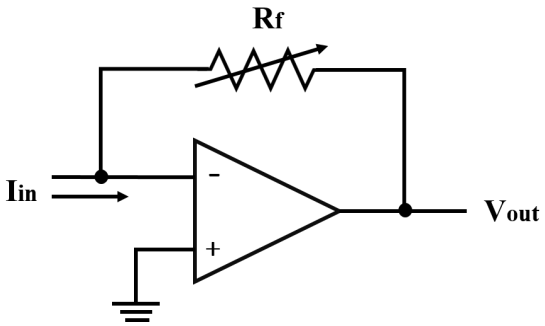


(a) Modulating input current with square wave of duty cycle of 1/M

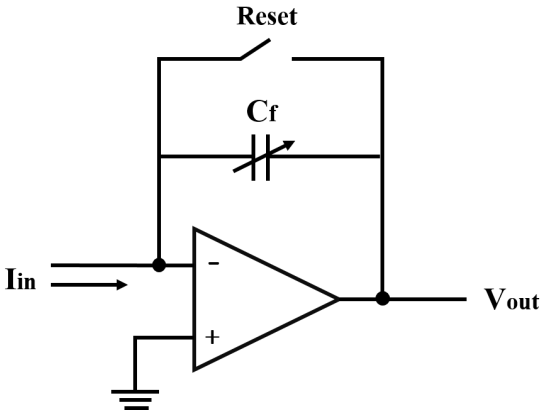


(b) System level diagram

Figure 2.5 Input-modulated $\Sigma\Delta$ based circuit. Reprinted from [8].



(a) Resistive feedback current readout circuit



(b) Capacitive feedback current readout circuit. The capacitor is reset in every clock cycle.

Figure 2.6 Voltage-mode circuit converts the bidirectional input current into voltage.

Resistive Feedback

Fig. 2.6a depicts a readout circuit which uses a transimpedence amplifier with feedback resistor, R_f to convert the input sensor current, I_{in} to voltage, V_{out}. The sensor current can be calculated by equation 2.3.

$$I_{in} = -\frac{V_{out}}{R_f} \tag{2.3}$$

The dynamic range of the current readout circuit can be tuned by varying R_f. The feedback resistor should be very large to reduce input noise. However, there is a trade-off between the chip area and noise since the on-chip R_f cannot be too large due to the constraints on chip area. The feedback resistor also generates thermal noise which limits the readout resolution.

Capacitive Feedback

A readout circuit with capacitive feedback can eliminate thermal noise introduced in resistive feedback. As shown in Fig. 2.6b, the readout circuit uses an operational amplifier that integrates the input sensor current, I_{in} to an output voltage, V_{out} at the capacitor, C_f. The input sensor current can be calculated by equation 2.4.

$$V_{out} = \frac{1}{C_f} \int_0^T I_{in} dt \tag{2.4}$$

where C_f is the feedback capacitor and T is the integration time. However, there are noise sources such as charge injection, clock feedthrough and KT/C noise in the feedback switch which limit the resolution of this readout circuit.

Switched-Capacitor

A switched-capacitor (SC) integrator readout circuit which utilises correlated double sampling (CDS) [11] can be introduced to eliminate the input offset error due to noise sources in the capacitive feedback readout circuit, thereby suppressing the noise at the output. The CDS technique involves sampling the input twice and recording their differences. It rejects slow-charging noise, and reduces 1/f noise, offset and other non-ideal effects inherent to CMOS amplifiers. An example of SC-integrator readout circuit [10] is shown in Fig. 2.7.

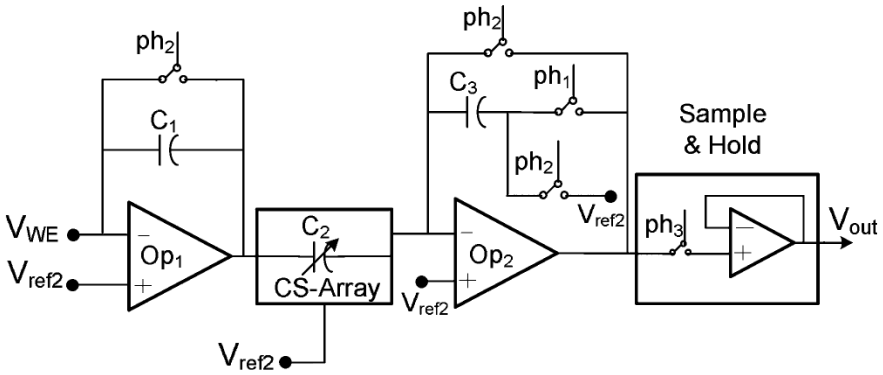


Figure 2.7 A typical switched-capacitor readout chain consists of an integrator followed by a PGA followed by a sample and hold. The capacitor is reset in every clock cycle. Ph1, P2, and Ph3 are non overlapping clocks. V_{ref2} is applied to the WE through OP1 to stimulate the sensor for CA or CV measurements. OP2, C3 and the capacitor array for the PGA. Reprinted from [10].

2.3.5 Current-mode Circuit

Current Conveyor

Another type of readout circuit that has been widely used is the current conveyor structure. A typical current conveyor schematic is shown in Fig. 2.8. The current conveyor readout circuit performs linear

operations and decoupling in current mode. The input current from working electrode can be measured by equation 2.5.

$$\frac{I_{in}}{I_{out}} = \frac{(W/L)_1}{(W/L)_2} \tag{2.5}$$

where I_{out} is the current conveyor output current and W/L is size of the current mirror transistor M1 and M2. Since there is no resistor or capacitor, the current conveyor can be very compact. However, it only allows input current in one direction. Offset current sources could be added to perform bidirectional current measurement.

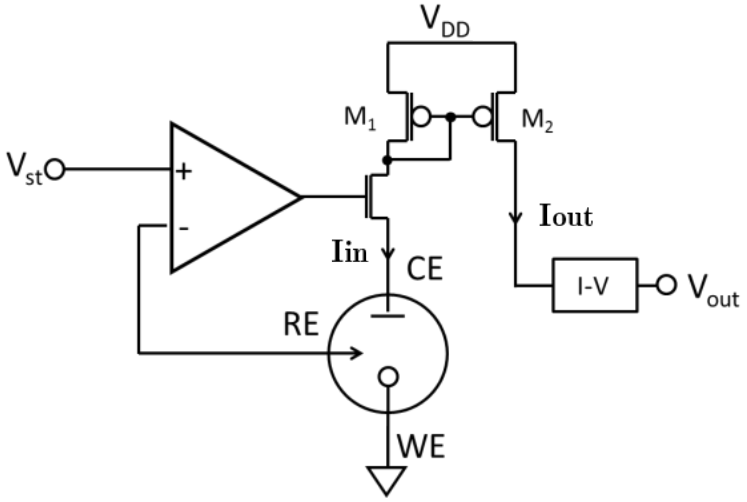


Figure 2.8 The structure of the typical current conveyor readout circuit with potentiostat. Reprinted from [3].

Current Preamplifier

Instead of using the typical current-to-voltage conversion obtained by means of resistive feedback transimpedance amplifier as discussed earlier, two double-MOS structures which consists of two couples of matched MOSFET transistors [12] can be used. The input current from WE is first amplified by the current preamplifier, then converted to an output voltage by a transimpedance amplifier. The transistors of the current preamplifier operates in the subthreshold region and are able to provide a wide linear current range. However, the authors did not present the simulation or measurement in detail. Thus, further analysis and simulation need to be carried out.

2.3.6 Comparison

The main characteristics of the state-of-the-art integrated readout circuits for amperometry biosensors are presented in Table 2.1. As it can be seen from the table, today's state-of-the-art integrated circuits for electrochemical detection still suffer from a lack of autonomy. This project aims to design the first integrated circuit that able to measure a wide dynamic range of input current autonomously.

	Circuit Structure	**Current Range**		**Dynamic**	**Autonomous**
		Min	**Max**	**Range**	**Gain**
TCAS'07[5]	Current to Time	1 pA	1 nA	60 dB	No
TBCAS'13[13]	Current to Frequency	24 pA	0.35 μA	83 dB	No
TBCAS'07[7]	Feedback modulated $\Sigma\Delta$	0.1 pA	$\pm$0.5 μA	134 dB	No
TBCAS'16[8]	Input modulated $\Sigma\Delta$	0.1 pA	16 μA	164 dB	No
TBCAS'17[14]	Switched-Capacitor	0.47 pA	$\pm$20 μA	153 dB	No
TCAS'13[9]	Current Conveyor	8.6 pA	$\pm$350 nA	92 dB	No
JCCS'09[15]	Current Preamplifier	1 fA	$\pm$ 1μA	180 dB	No
Target Design		1 pA	1 μA	120 dB	Yes

Table 2.1 Comparison between state-of-the-art of the amperometric current readout circuits

Chapter 3

Initial Architecture

The preliminary choices on the readout circuit structure are narrowed down and presented in Table 3.1. They are chosen because of their wide linear current range, wide dynamic range and also the simplicity of the circuit which allow easier integration with autonomous gain control. The readout circuits as presented in Table 3.1 also allow bidirectional current measurement.

	Circuit Structure	Complexity	Linear Current Range	Input Dynamic Range
JSSC'09[15]	Current Preamplifier	Low	1 fA - $\pm$1 μA	180 dB
TBCAS'17[14]	Switched Capacitor	Medium	0.47 pA - $\pm$20 μA	153 dB

Table 3.1 Comparison between preliminary choices of readout circuits

The current preamplifier based on the work of G.Ferrari [15] is chosen as the initial architecture of the readout circuit for the project since it claims to provide a wide dynamic range. The use of the double-MOS structure also reduces the chip area significantly. However, simulations need to be carried out to confirm these. All the implementations and simulations were carried out in the **GPDK 180nm** technology. The switched-capacitor architecture is also implemented and simulated to make comparison with the current preamplifier before making decision on the final readout circuit architecture.

3.1 Current Preamplifier

The matched double-MOS structure is the core architecture of the current preamplifier as illustrated in the blue box of Figure 3.1. The characteristics of the double-MOS structure are listed below:

- Consists of both NMOS and PMOS transistors. This structure allows bidirectional input current flow. The direction of current flow is illustrated in Fig. 3.2.
- The transistors have the exact same gate-drain voltages, V_{DS} and gate-source voltages, V_{GS}. Hence, they always work in the same operating region.

- The transistors operate in subthreshold region by connecting the gate of the transistors to half of the VDD.

The device width of the second double-MOS structure is larger than that of the first double-MOS structure by factor of N. Since both of the double-MOS structures have the same drain and source voltage, thus the output current which flows in second double-MOS structure is amplified by factor of N as well. The drain current across the device can be expressed in the equation 3.1 by recalling the drain current in subthreshold region.

$$i_{D(subthreshold)} = \frac{W}{L}\mu_e C_{ox}\left(\frac{kT}{q}\right)(n-1)e^{\frac{V_{GS}-V_T}{nkT}}(1-e^{\frac{-qV_{DS}}{kT}}) \tag{3.1}$$

By operating in the subthreshold region, the double-MOS contributes a very small shot noise and flicker noise that scale accordingly with the input current. The total power consumption is also very low as low current is drawn.

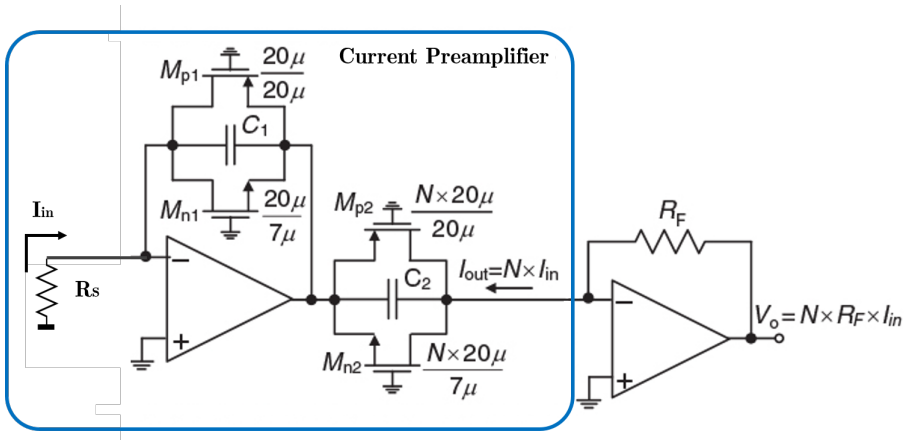
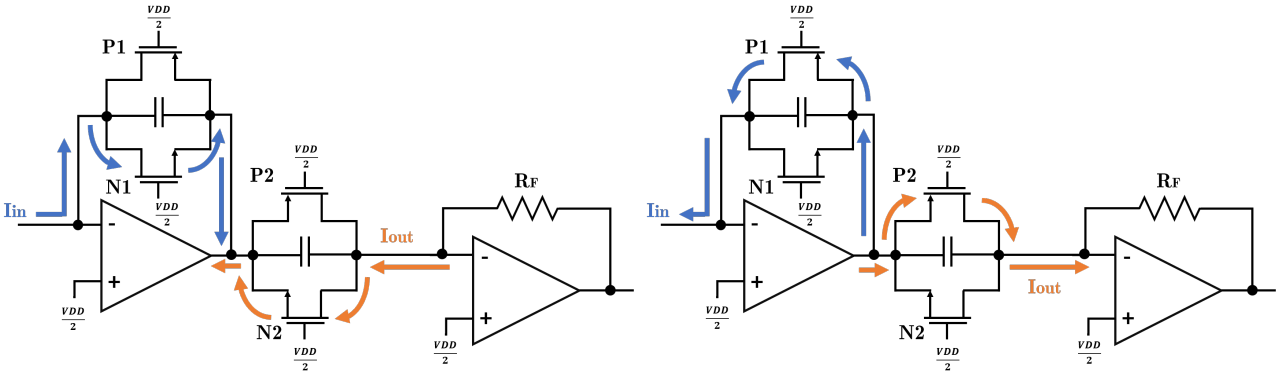


Figure 3.1 Proposed scheme of current preamplifier. Reprinted from [15].



(a) Input current flows away from WE

(b) Input current flows into WE

Figure 3.2 Bidirectional input current flow into or out of the current amplifier. The direction of the input and output currents are opposite.

3.1.1 Small-Signal Analysis

The current preamplifier is modelled in a small-signal model as shown in Fig. 3.3. Small-signal analysis was carried out to verify the relationship between the output current I_{OUT} and the input current I_{IN}. R_s represents the sensor resistance where the input current flows.

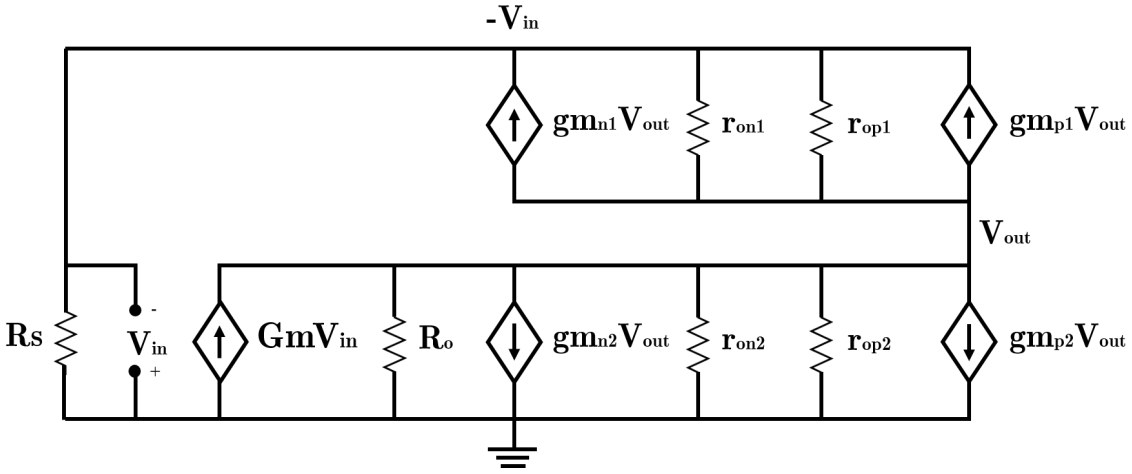


Figure 3.3 Small-signal model of the current preamplifier from the blue box of Fig. 3.1

$$I_{in} = gm_{n1}V_{out} + gm_{p1}V_{out} + \frac{V_{in} - V_{out}}{r_{on1}||r_{op1}} \tag{3.2}$$

$$I_{in} = \frac{V_{in}}{R_s} \tag{3.3}$$

Equate (3.1) and (3.2) yield:

$$A_V = \frac{V_{out}}{V_{in}} = \frac{\frac{1}{R_s} - \frac{1}{r_{on1}||r_{op1}}}{gm_{n1} + gm_{p1} - \frac{1}{r_{on1}||r_{op1}}} \tag{3.4}$$

Output current is given by:

$$I_{out} = GmV_{in} - gm_{n2}V_{out} - gm_{p2}V_{out} - \frac{V_{out}}{r_{on2}||r_{op2}||R_o} \tag{3.5}$$

$$I_{out} = GmI_{in}R_s - gm_{n2}I_{in}R_sA_v - gm_{p2}I_{in}R_sA_v - \frac{I_{in}R_sA_v}{r_{on2}||r_{op2}||R_o} \tag{3.6}$$

$$\frac{I_{out}}{I_{in}} = GmR_i - R_s\left(\frac{\frac{1}{R_s} - \frac{1}{r_{on1}||r_{op1}}}{gm_{n1} + gm_{p1} - \frac{1}{r_{on1}||r_{op1}}}\right)\left(gm_{n2} + gm_{p2} + \frac{1}{r_{on2}||r_{op2}||R_o}\right) \tag{3.7}$$

Let $gm_1 = gm_{n1} + gm_{p1}$, $gm_2 = gm_{n2} + gm_{p2}$, $r_{o1} = r_{on1}||r_{op1}$ and $r_{o2} = r_{on2}||r_{op2}$

Since N2 and P2 consist of N replicas of N1 and P1, $gm_2 = Ngm_1$ and $r_{o2} = \frac{r_{o1}}{N}$. Equation (3.7) is simplified to:

$$\frac{I_{out}}{I_{in}} = GmR_s - R_s\left(\frac{\frac{1}{R_s} - \frac{1}{r_{o1}}}{gm_1 - \frac{1}{r_{o1}}}\right)\left(Ngm_1 + \frac{1}{\frac{r_{o1}}{N}||R_o}\right) \tag{3.8}$$

$$\frac{I_{out}}{I_{in}} = GmR_s - \left(\frac{r_{o1} - R_s}{gm_1 r_{o1} - 1}\right)\left(\frac{N(1 + gm_1 r_{o1})}{r_{o1}}\right) \tag{3.9}$$

Assuming $gm_1 r_{o1} >> 1$, this gives the relationship between I_{in} and I_{out} as:

$$\frac{I_{out}}{I_{in}} = -N + R_s\left(Gm + \frac{N}{r_{o1}}\right) \tag{3.10}$$

Referring to equation 3.10, the first term represents the desired relationship where output current is amplified by a factor of N. However, the second term is undesirable since it adds an offset which is based on the sensor resistance of the working electrode. Simulation is carried out to determine its effects on the linearity between the input and output current.

3.1.2 Transconductance Amplifier

Folded cascode topology has been chosen as the operational amplifier in the current preamplifier because it provides high gain and stability for big load. It is also able to achieve a good tradeoff between noise, output range, and power performance. The input stage consists of PMOS with large area to reduce the flicker noise. The characteristics of the folded cascode amplifier are shown in Table 3.2.

Parameter	Values
Gain (dB)	78
-3db Bandwidth (kHz)	6.5
Phase Margin ($^\circ$)	42.8
Power Consumption (mW)	1.58
CMRR (dB)	106.3
PSRR (dB)	45.2

Table 3.2 Folded cascode amplifier characterisation

3.1.3 Circuit Level Simulation

A simulation is carried out where the sensor resistance, R_s at the inverting input of the operational amplifier is swept to generate an input current ranging from 1pA to 1 μA to represent the current flows in the WE. The simulation setup is shown in Fig. 3.5. The amplification factor, N is fixed at 10.

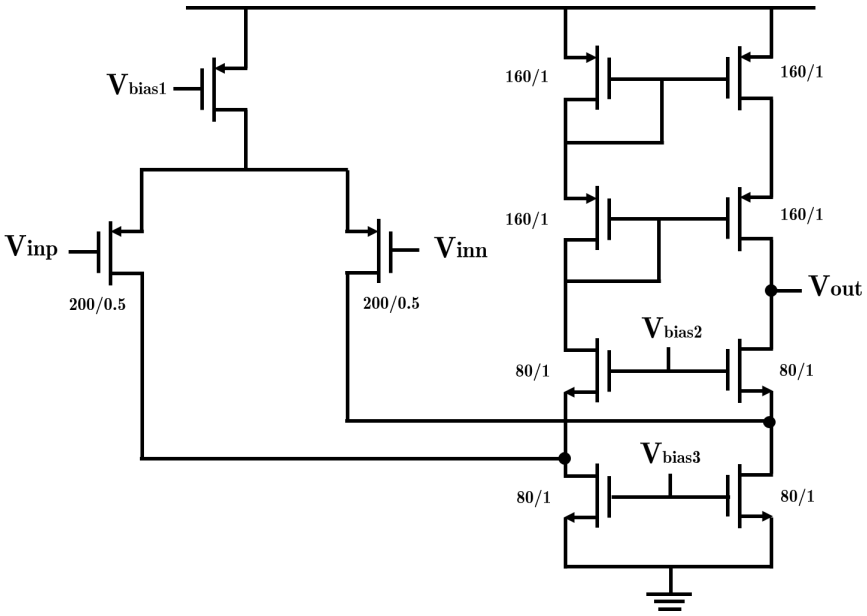


Figure 3.4 Schematics of folded cascode OTA

I_{out}/I_{in} is plotted against sensor resistance in Fig. 3.6 to verify equation 3.10 derived in the previous section. Values obtained from equation 3.10 is plotted in the same graph by using typical values of the parameters as shown in Table 3.3 to allow for comparison. Based on the results in Fig. 3.6, for very large R_s ($> 10^8\Omega$) or very small input currents, the second term in Eq. 3.10 becomes significant and hence create an upward slope which affects the gain factor.

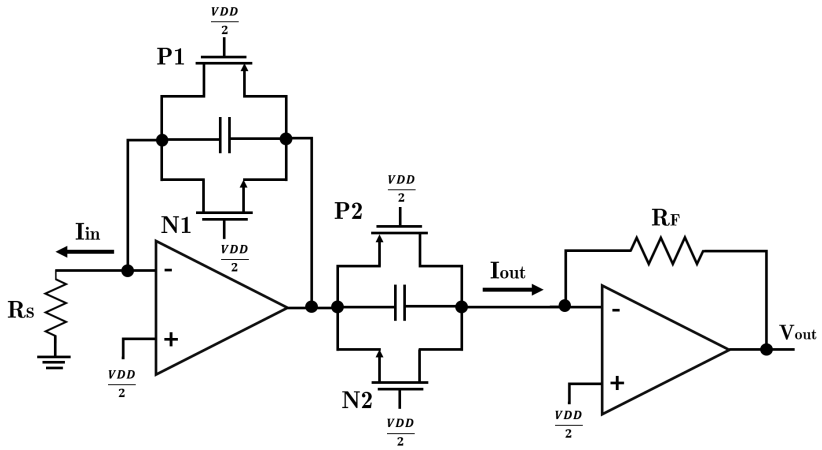
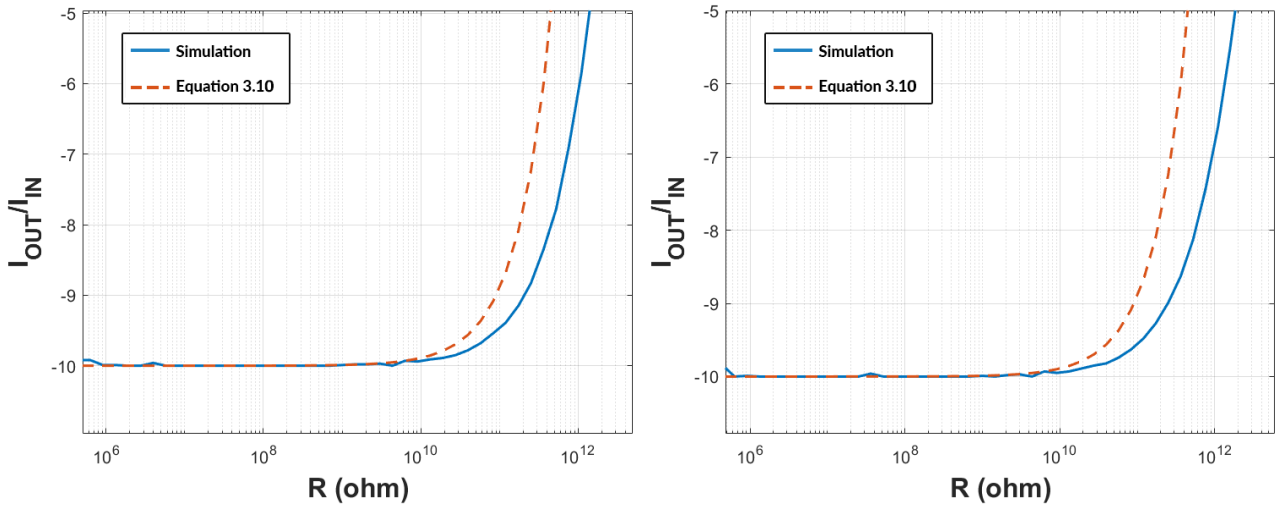


Figure 3.5 Simulation setup for current preamplifier.

The maximum and minimum input current are determined by a 1 % deviation from N, which is 10 in this case. For current flowing away from the WE, the input current range is between **47.2 pA and 1.2 μA** whereas for current flowing into WE, the input current range is between **47.2 pA to 1.85 μA** as illustrated in Fig. 3.7. The maximum input current is limited by the maximum output current of the amplifier while the minimum input current is limited by the undesirable sensor resistance effect.

Gm	N	r_o (subthreshold)
2 mA/V	10	$10^{12}\ \Omega$

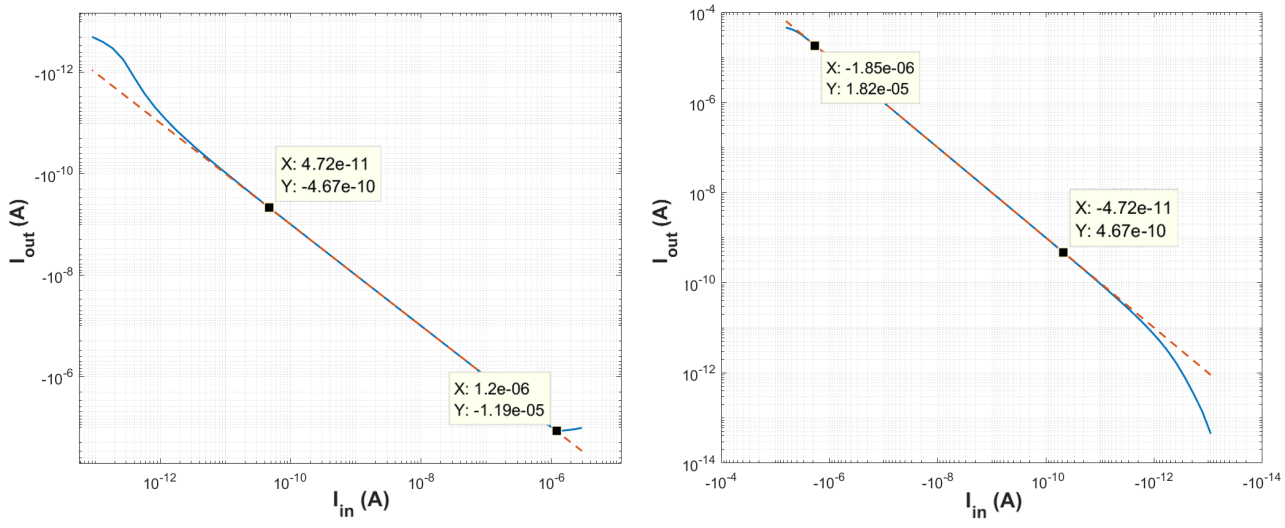
Table 3.3 Typical parameter value in equation 3.10



(a) Input current flows away from the WE

(b) Input current flows into the WE

Figure 3.6 The simulation result (blue) shows I_{OUT}/I_{IN} increases as the sensor resistance increases. In other words, the output current is no longer linear at low input current. The result is corresponding to line plotted using Equation 3.1 (orange).

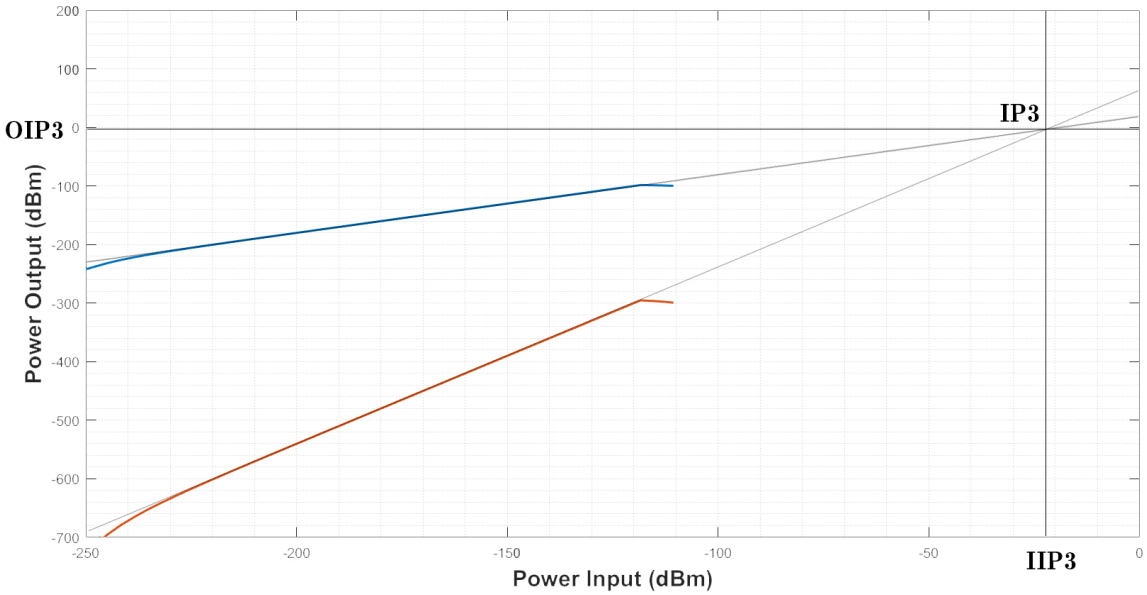


(a) Input current flows away from WE

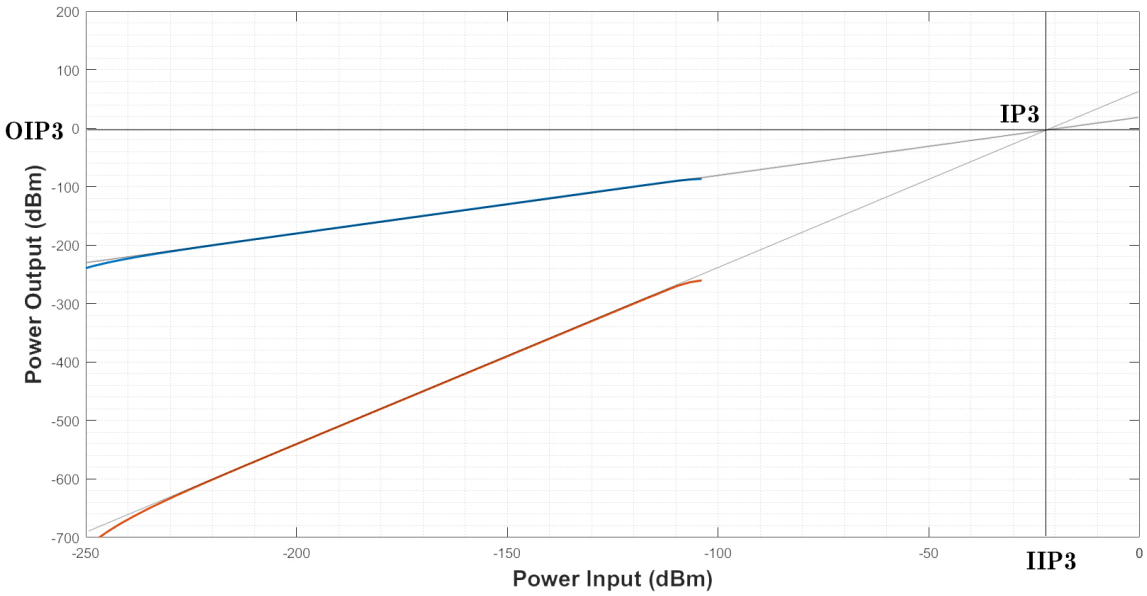
(b) Input current flows into WE

Figure 3.7 Graph of I_{OUT} against I_{IN} from the simulation results (blue). The maximum and minimum input current range is determined by 1 % deviation from the calculated value (orange).

The output current exhibits a linear relationship with the input current. However, there are distortions at both high and low input current. The non-linearity of the relationship is quantised using the Third-order intercept (IP3 or TOI)[16] as shown in Fig. 3.8. The IP3 points are the same regardless of the direction of current flow. The current preamplifier has an IP3 rating of -1 dBm with reference to the output axis and rating of -23 dBm. It indicates a fairly good linearity since the preamplifier can process 23 dBm of input signal before reaching the intermodulation distortion.



(a) Input current flows away from the WE



(b) Input current flows into the WE

Figure 3.8 Third-order intercept for quantising the non-linearity of the current preamplifier.

The output current from the current preamplifier is converted into voltage by adding a transimpedance amplifier at the output stage and then converted to a digital output using ADC. In order to produce a detectable output voltage, small current should be amplified for a few times to generate a larger current. Hence, the current preamplifiers are then cascoded together to create gain settings in multiples of 10 as shown in Fig. 3.9. Based on the simulation result in Fig. 3.10, the current preamplifier stages only able to amplify the bidirectional input current ranges between **62.3 pA and 1 μA** with less than 1% error. The lower limit of the dynamic range of the input current is worse compared to the single stage current preamplifier due to the cumulative effect of the cascode. Other possible sources of non-idealities such as offset voltage of the folded cascode OTA that introduces different operating points to the first and second double-MOS structure need to be investigated and rectified to ensure the current preamplifier exhibits high linearity across the dynamic range and down to 1 pA.

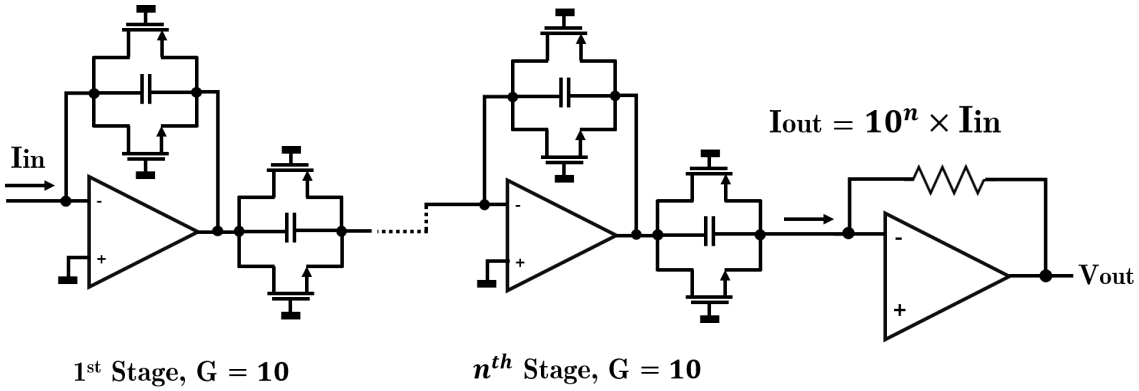


Figure 3.9 Simulation setup for cascoded current preamplifier for different gain settings.

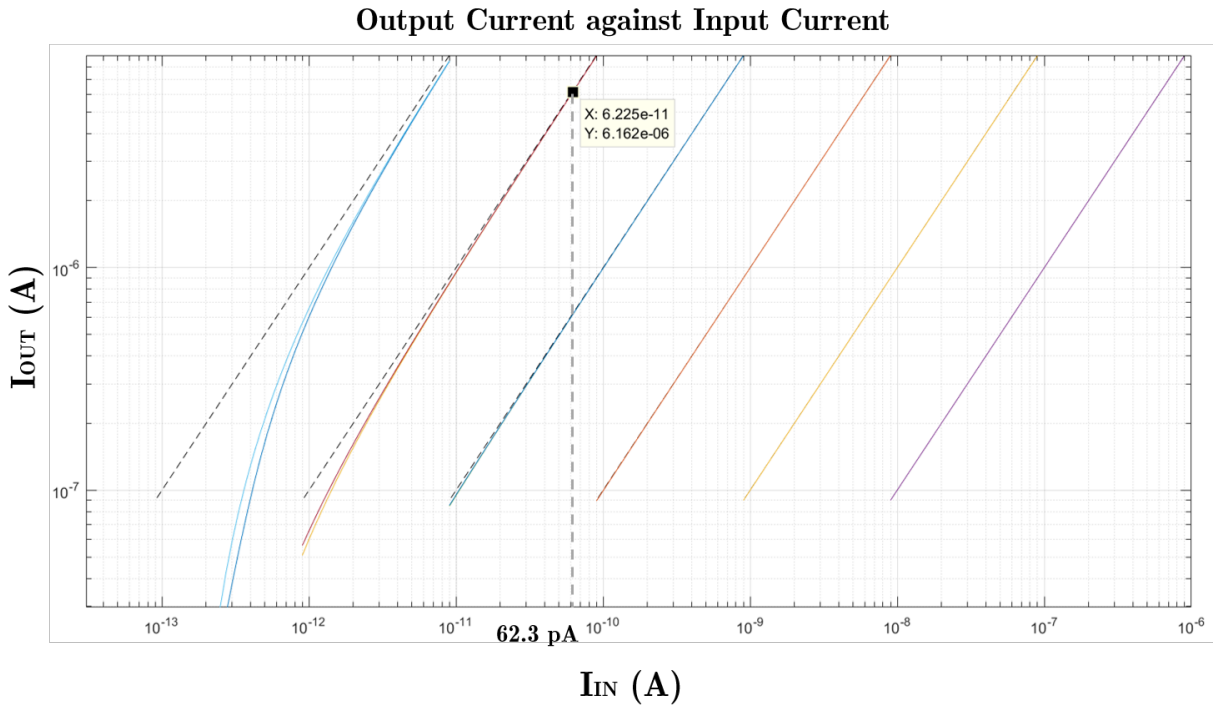


Figure 3.10 Output current against input current for different gain settings where the dashed lines represent the ideal values of I_{OUT}. There are large deviation for I_{IN} less than 62.3 pA.

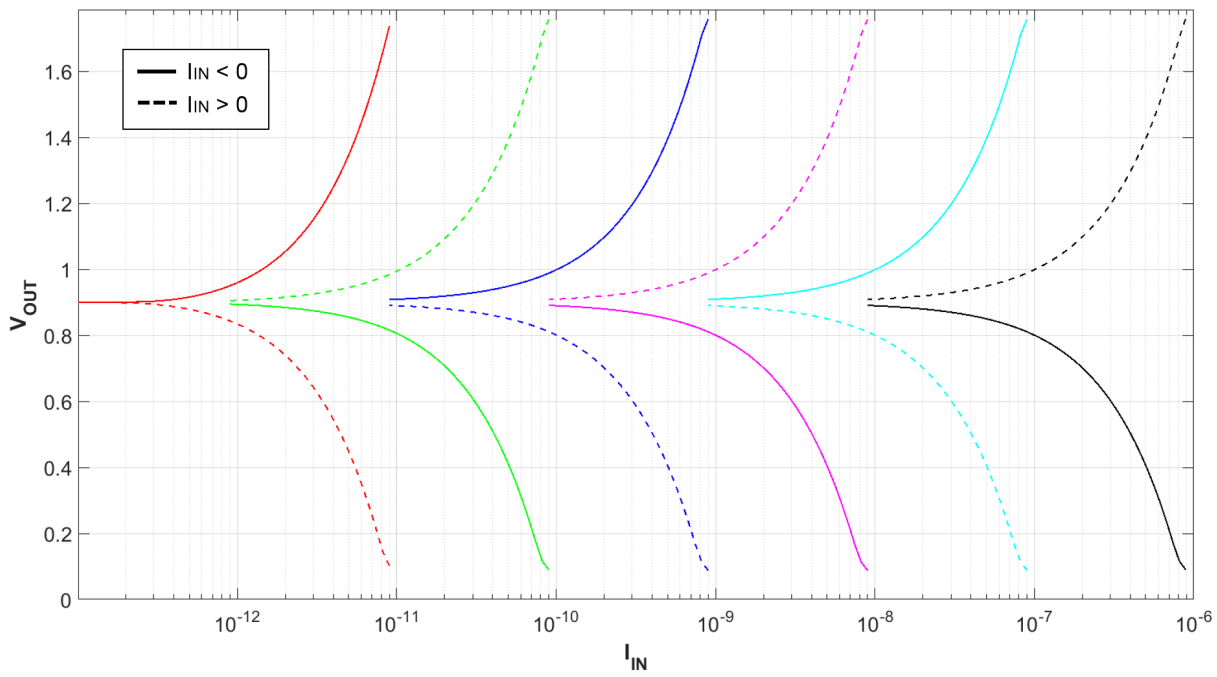


Figure 3.11 Output voltage against input current for different gain settings.

3.2 Switched-Capacitor Integrator

As mentioned in the previous section, there were gain error and offset in amplifying the current especially at extremely low current which affect the linearity. Hence, it limits the dynamic current range of the readout circuit. The switched-capacitor topology is then investigated. To make a fair comparison with the current preamplifier, the switched-capacitor integrator is implemented using the same folded cascode amplifier used in the current preamplifier with the same power consumption, transconductance and output current. A simple switched-capacitor integrator is designed and shown as Fig. 2.6(b). It consists of a folded cascode amplifier, a reset switch and an integrating capacitor.

3.2.1 Circuit-Level Simulation

A similar transient simulation is carried out where a resistor, R_s is placed at the inverting input of the folded cascode amplifier to generate an input current which represents the current flows in the WE. The switched-capacitor integrator converts the input current directly into voltage. The relationship between output voltage and input current is given by:

$$V_{out} = \frac{1}{C_{int}} \int_0^{\frac{T_{clk}}{2}} I_{in} dt + V_{cm} \tag{3.11}$$

$$V_{out} = \frac{T_{clk} I_{in}}{2C_{int}} \tag{3.12}$$

where T_{clk} is the period of the reset clock with 50% duty cycle, C_{int} is the integrating capacitance and V_{cm} is the common mode voltage which is 900 mV in this case.
However, there are also two main sources of error [14] in switched-capacitor which are

1. the **finite transconductance**, G_m of the folded cascode transconductance amplifier which causes the input differential voltage of opamp increases when the input current to increase. This effect needs to be eliminated to keep the output voltage as accurate as possible.

2. the **on-resistance**, r_{on} of the low leakage switch which prevents the full discharge of the capacitor during reset.

The relationship of V_{out} and I_{in} is shown in equation 3.13 by considering the effects of the two error terms that are previously mentioned.

$$\frac{V_{out}}{I_{in}} = \frac{T_{clk}}{2C_{int}} + r_{on} - \frac{1}{G_m} \tag{3.13}$$

The maximum input current of the switched-capacitor integrator is only 1.75 μA it is limited by the high on-resistance of the switch which creates large voltage drop across it. When input current of 1 μA is fed into the circuit, an output voltage is exactly the same as the expected value. However, for an input current less than 10 pA, the output voltage begins to deviate more than 1%. Based on the transient simulation in Fig. 3.13, the output voltage gives a deviation of 1.25 % which is due to

the presence of leakage current in the switch. Nevertheless, this topology still gives a wider dynamic range compared to that of the current preamplifier. The dynamic range can be expanded further by increasing the output voltage of the opamp and replacing the switch with a low-leakage switch.

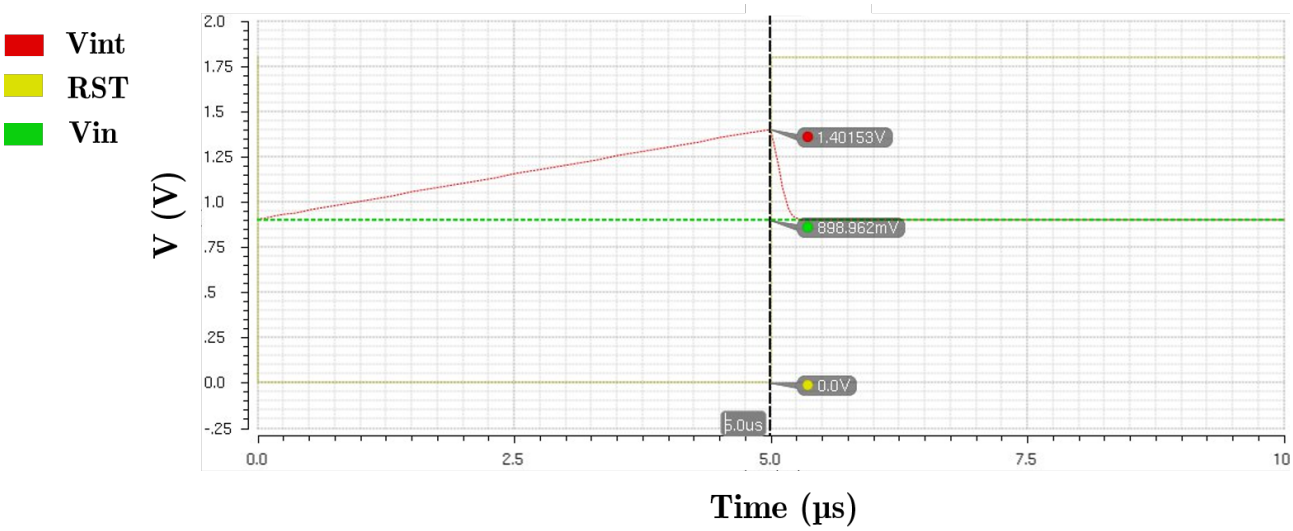


Figure 3.12 Output voltage of the switched-capacitor for an input current of 1 μA integrated at 10 pF capacitor for 5 μs. The output voltage is 1.40 which is same as the calculated value.

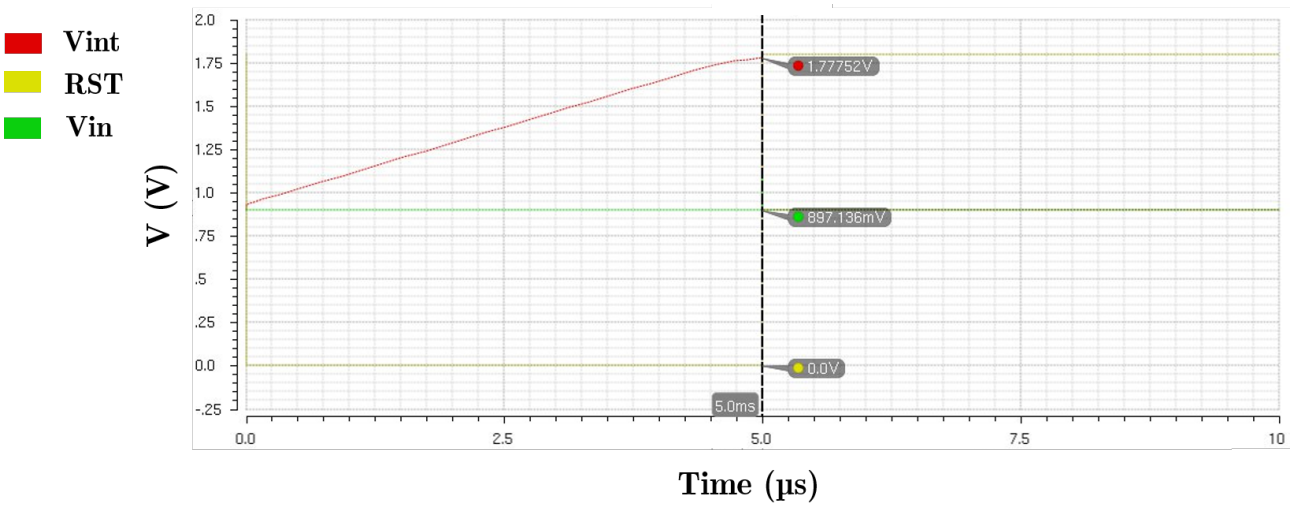


Figure 3.13 Output voltage of the switched-capacitor for an input current of 10 pA integrated at 50 fF capacitor for 5 ms. The output voltage is 1.7775 V and the deviation is 1.25% from the calculated value.

3.3 Comparison

Finally, a comparison between the current preamplifier and switch-capacitor integrator is made and illustrated in Table 3.4. The latter is chosen as the topology for the readout circuit as it is able to offer a wider dynamic input current range. It is also more immune to noise and has a smaller area.

Topology	**Current Preamplifier**	**Switched-Capacitor Integrator**
Operation	Input current is amplified by the current preamplifier and then converted into voltage by a transimpedance amplifier	Input current is converted directly into current at the capacitor
Mode settings	Requires stages of current preamplifiers	Only requires different combinations of integrating frequencies and capacitance
Area	Larger due to multiple opamps for different mode settings	Smaller because only one opamp is required for mode settings
Dynamic Range	62.3 pA - 1.18 μA Lower limit is limited by offset caused by sensor resistance as expressed in (3.10) Upper limit is limited by finite transconductance of opamp	10 pA - 1.75 μA Lower limit is limited by leakage current in the reset switch Upper limit is limited by on-resistance of the switch

Table 3.4 Comparison between current preamplifier and switched-capacitor integrator

3.4 Chapter Summary

The current preamplifier is designed and its performance is simulated. It gives a fairly good performance in amplifying the current. However, it suffers from non-linear distortion at very low input current less than 47 pA. Based on the small-signal analysis and the simulation result, an offset is contributed by the sensor resistance from the working electrode which affects the linearity between the input and output current. This is a undesirable characteristic for a analogue sensing circuit. The limitations of the current preamplifier lead to the implementation of a switched-capacitor architecture. A simple switched-capacitor is implemented and designed using the same opamp as the current preamplifier. It shows a significant improvement in the permissible dynamic range. Thus, it is chosen as the analogue part of the readout circuit. However, there is still room of improvement for this topology; for example, replacing the switch with a low-leakage switch. Its implementation process is explained in detail in the next chapter.

Chapter 4

Analogue Circuit

As described in the previous chapter, the current preamplifier suffers from non-linear distortion at low input current. Its dependence on the sensor resistance is also undesirable. Therefore, the employment of a switched-capacitor architecture will be the main focus in this chapter. Its implementations along with design justifications will be described in the following sections.

The target design specifications of the analogue circuit are listed below:

1. **Wide dynamic range** of input current preferably from 1 pA to 1 μA or even beyond the limits. This characteristic can ensure that the readout circuit is able to measure different ranges of current from different metabolites (such as glucose and lactate).

2. **High linearity**. The current integrated at the capacitor should increase linearly with integration time, so that the output voltage is very close to the ideal value obtained from the formula V = It/C.

3. **Low noise**. Thus, the readout circuit can have low minimum detectable current and higher accuracy especially in capturing very low input current.

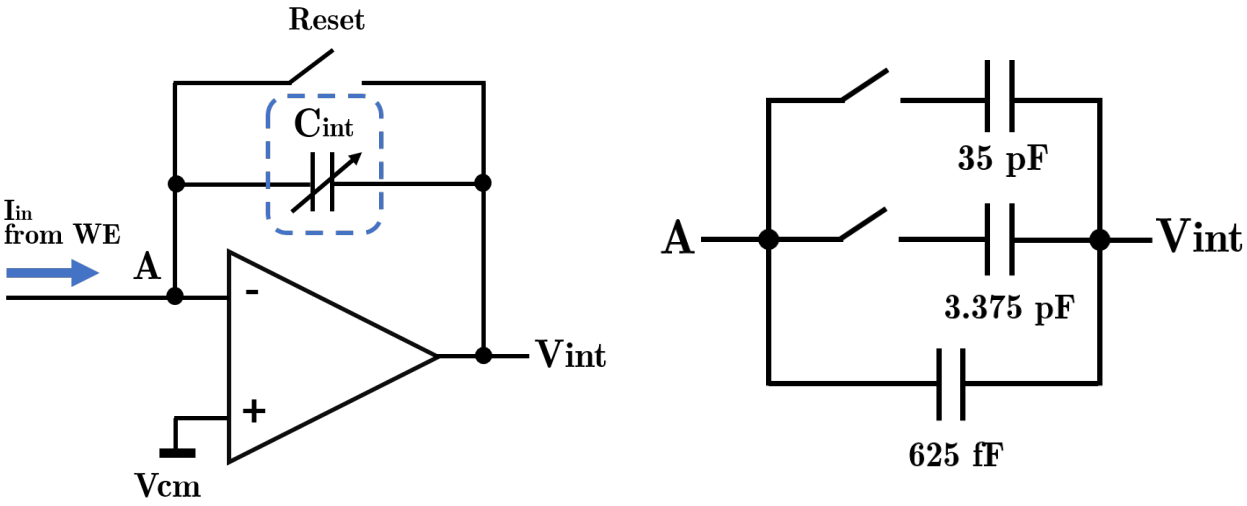
4. **Low power consumption** for power-savings. Static power consumption which typically comes from leakage current, and dynamic power consumption from charging and discharging of capacitive node should be optimised.

In this chapter, the implementations and simulations were carried out in **AMS 350nm** technology instead of GPDK 180 nm in the previous chapter to allow more voltage headroom during the implementation process.

4.1 Switched-Capacitor Integrator

The switched-capacitor integrator as shown in Fig. 4.1a consists of a differential folded cascode amplifier, integrating capacitors and switches. As mentioned in previous chapter, a folded cascode topology is chosen because it provides high gain and stability for a big load. As shown in Fig. 4.2,

large transistors are used for the input differential pair to limit noises such as flicker noise and mismatch which could affect the linearity of the integrating current. The dimensions of the transistors are chosen carefully to ensure they are deep in saturation operating region and work properly under different modes and input current range. The maximum output current of the transconductance amplifier is set close to the maximum input current from the WE to reduce the power consumption. The characteristics of the amplifier is presented in Table 4.1. A reset switch is also added in parallel to the capacitor so that the integration time can be defined. When the switched is opened, the current flows through the capacitor and generate an output voltage, V_{int}. When the switch is closed, the current flows through the switch and thus the current is no longer integrated at the capacitor.



(a) Switched capacitor integrator. The blue dashed block is the capacitor array.

(b) Capacitor Array

Figure 4.1 Switched capacitor integrator

Parameter	Values
Gain (dB)	92
-3db Bandwidth (kHz)	7.5
Phase Margin (°)	44.8
Power Consumption (mW)	2.39
Max. Output Current (μA)	14
CMRR (dB)	130.4.3
PSRR (dB)	82.2

Table 4.1 Folded Cascode amplifier characterisation

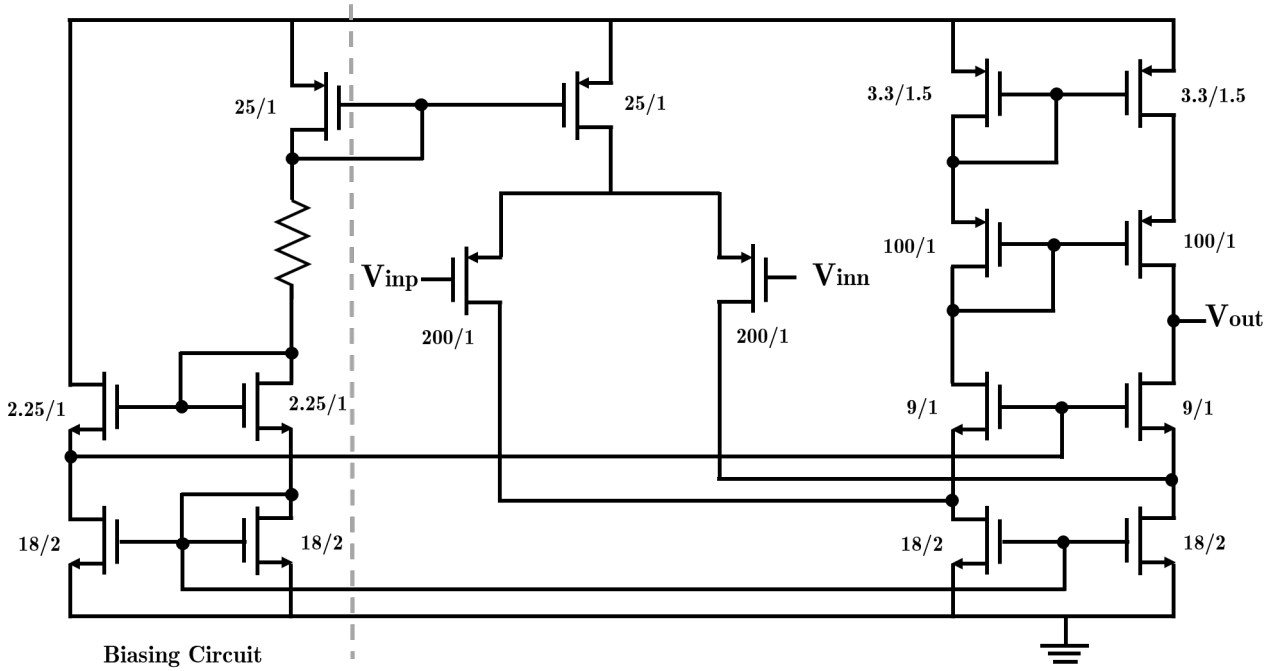


Figure 4.2 Schematic of folded cascode amplifier

The capacitor array consists of 3 capacitors with their corresponding switches, together with different integration times, thus enabling different operating modes to measure the input current with a wide dynamic range. Based on Fig. 4.1b, the smallest capacitor in the array is 625 fF and it is always conducting at all operating modes. Larger capacitors, 3.375 pF and 35 pF only conduct at modes which integrate higher current. For example, all three capacitors are only conducted and connected in parallel to produce a resultant capacitor of 40 pF to integrate input current above 1 μA. The advantages of this arrangement of the capacitor array with switches are area savings and high accuracy. The total silicon area occupied by this arrangement is less compared to that of arrangement with 3 capacitors of 40 pF, 5 pF and 625 fF with their respective switches. In addition, there is no switch across the smallest capacitor which would otherwise cause potential distortion at the integrating capacitor at a very low current.

4.2 Low-Leakage Switch

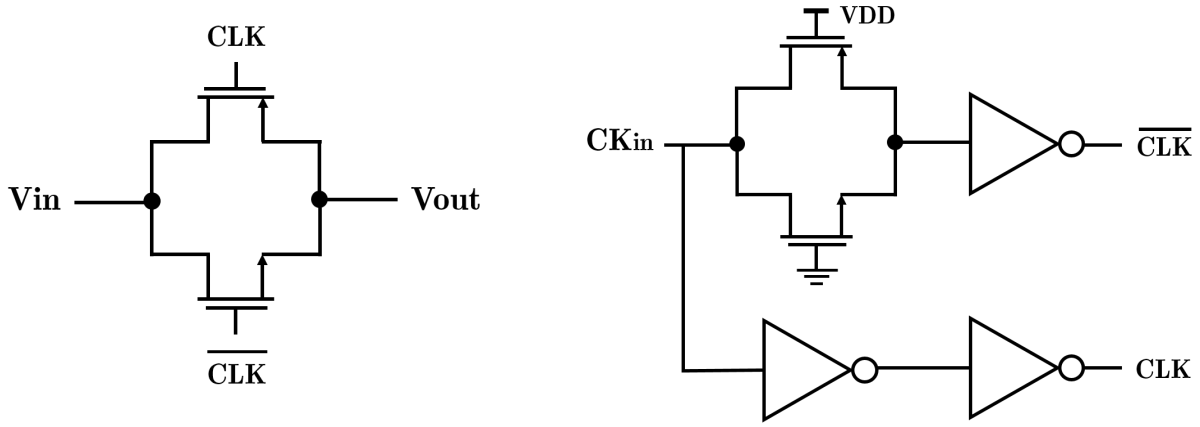
The switches of the switched-capacitor have to be designed carefully as they need to limit voltage drop and charge injection. The complementary switch [17] as illustrated in Fig. 4.3 has been chosen because it can offer many advantages; firstly, with proper sizing, it can operate as a small resistor when it is turned off. The equivalent resistance of the switch is given by:

$$R_{eq} = \frac{1}{m_n C_{ox}(\frac{W}{L})_N (V_{DD} - V_{THN})[m_n C_{ox}(\frac{W}{L})_N - m_p C_{ox}(\frac{W}{L})_P]V_{in} - m_p C_{ox}(\frac{W}{L})_P} \tag{4.1}$$

Referring to equation 4.1, if the condition in 4.2 is satisfied, then the on-resistance of the switch is independent of the input voltage level. Thus, there is much lesser variation contributed by each switch alone.

$$m_n C_{ox}\left(\frac{W}{L}\right)_N = m_p C_{ox}\left(\frac{W}{L}\right)_P \tag{4.2}$$

Secondly, the charge injection from the switch is also limited. This is because the complementary switch consists of both the PMOS and NMOS, thus they are able to inject opposite charges which cancel out each other when the switch is turned off. Lastly, it only consists of two transistors, thus it can effectively reduce the area. To further improve the performance of the switch in term of speed, delay elements in Fig. 4.3b are added to synchronise the clocks, so that both MOSFET can be turned off simultaneously. However, when the switched-capacitor integrator is at low current mode, the integrated voltage is less than that of the ideal voltage. This is due to the presence of small leakage current that flows through the off-switch. Although the effect of the leakage current is only noticeable when integrating very low current, modifications should be made on the switch to rectify this problem since the readout circuit is expected to operate below 1 pA.



(a) Topology

(b) Delay element is added

Figure 4.3 Complementary switch. Adapted from [17]

A reset switch is also required to reset the capacitor of the integrator after the sample period and define the integration time. Thus, a low-leakage switch [18] is introduced for both reset switch and switches in capacitor array. The switch is extremely important to limit the voltage drop rate in the switched capacitor integrator and hence, improving the accuracy of the integrated input current. The low-leakage switch structure is implemented based on the floating-body techniques in which an extra lateral transistor, M3 was employed to reduce the leakage as shown in Fig. 4.4. The leakage current is compensated by transistor M3. When transistors M1 and M2 are turned off, their drain leakage current flows in the current path introduced by M3. At the same time, node B of the low leakage switch in Fig. 4.4 is kept at Vcm, thus almost no potential difference exists between node A in Fig. 4.1 between node B in Fig. 4.4, hence current flow is limited.

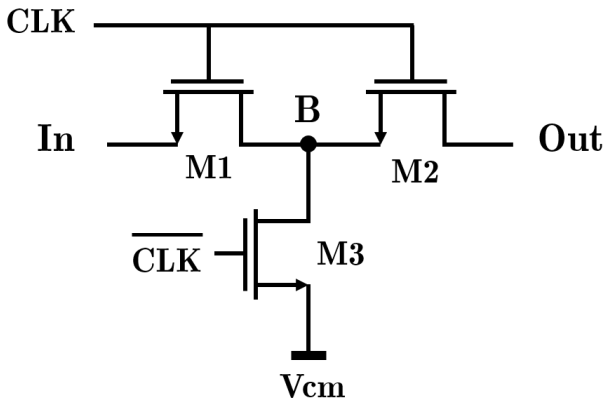


Figure 4.4 Low Leakage Switch

4.3 Sample and Hold Circuit

The input current is converted into voltage by the integrator at the first stage and this voltage should be sampled and its value should be stored for a period of time until the next sample stage. A simple switched-capacitor sample and hold circuit as depicted in Fig.4.5 is first implemented. Correlated double sampling [19] technique is introduced to produce output with reduced noise and offset from the signal. However, this topology resets to the common mode voltage at each clock period and thus requires an opamp with high slew rate. There is also a voltage drop across long hold time for this topology.

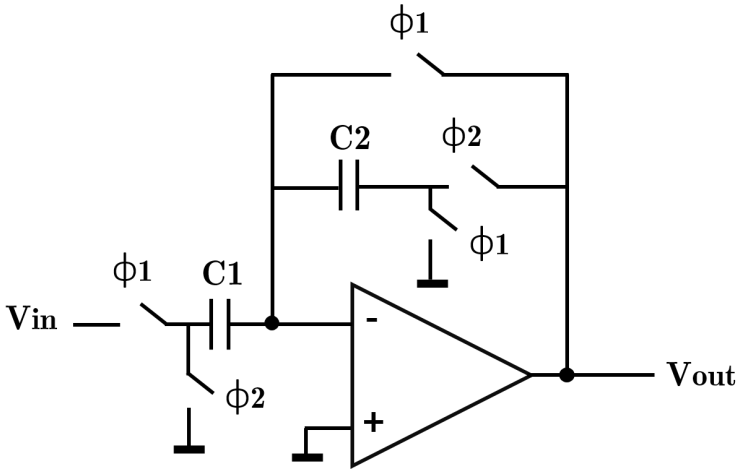


Figure 4.5 Initial sample and hold circuit. Reprinted from [19]

A wide-band offset compensated sample and hold circuit [19] is then implemented as shown in Fig. 4.6. Anticipatory compensation is introduced in this topology by pre-charging the capacitor, C3 with voltage which is expected during the next stage. Hence, slew rate and settling time can be relaxed. The frequency dependence of the voltage gain of the compensated amplifier can be reduced, and thus

the operation of the circuit can be stable at high frequency.

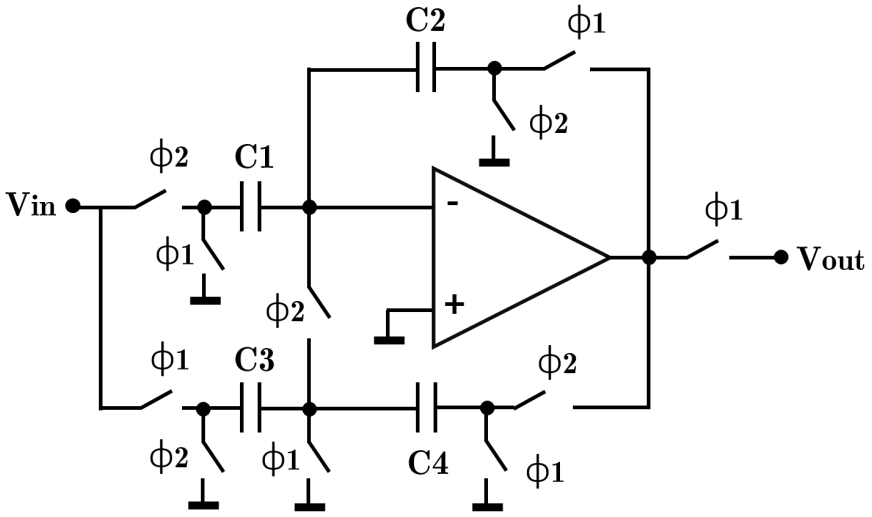


Figure 4.6 Sample and hold circuit. Reprinted from [19]

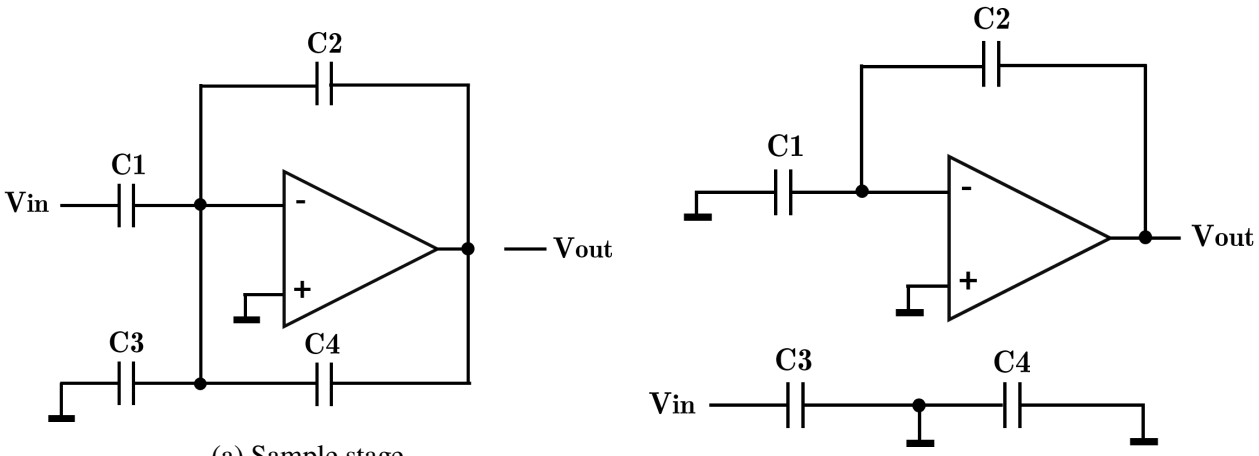


Figure 4.7 The operation of sample and hold circuit

At high current, there is a small offset at the inverting input of the opamp in the switched-capacitor integrator. To compensate this effect, the offset is sampled and deducted from the output voltage from the integrator. Hence, the output voltage from the sample and hold circuit is free from the offset.

4.4 Comparator

Comparators are used to compare the output voltage from the sample and hold circuit with the reference voltage, so that the digital circuit can change the operating mode of the readout circuit based on

the magnitude of input current. Since comparator is only needed after the integration, a clocked comparator [20] in Fig. 4.8 can be used to reduce the power consumption. The clocked comparator consists of the sense amplifier at the left hand side and NAND gate latch at the right hand side.

The sense amplifier [20] consists of latch formed by transistors M1 - M4. When the clock is low, all the nodes in the circuit are either pulled to VDD or ground due to the latch. This action therefore erases all the previous memory of each nodes of the comparator which is a good characteristics for a comparator. When clock goes high, the two inputs are compared causing the output of the circuit to register which one is higher.

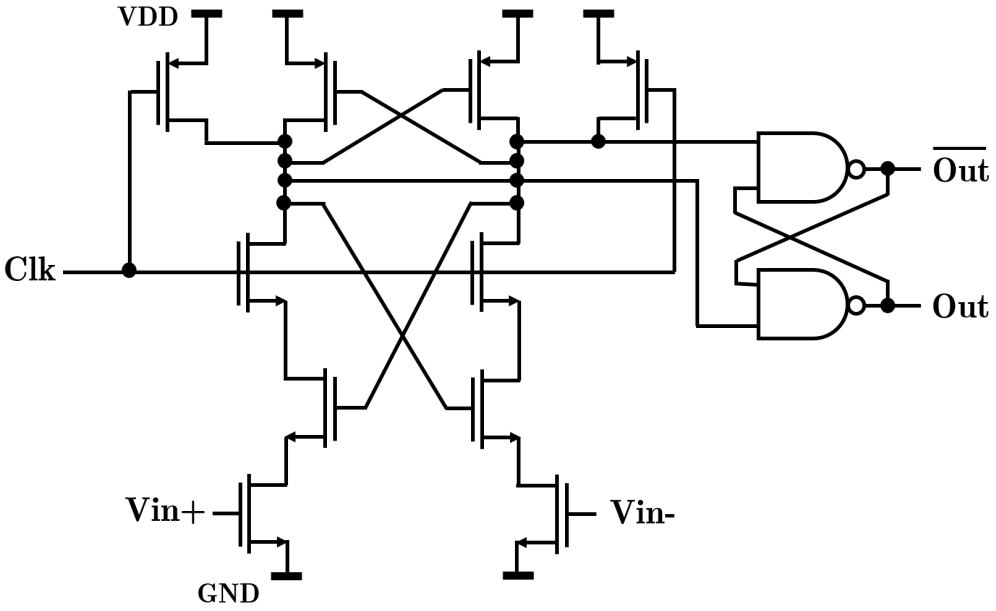


Figure 4.8 Clocked comparator. Reprinted from [20]

4.5 Analogue-To-Digital Converter

An analogue-to-digital converter is required at the output of the sample and hold stage to provide a digital output which is proportional to the measured current. A 10 bit-SAR ADC from the AMS Analogue standard cell library is used since it is able to provide up to 10-bits resolution and only occupy a small area.

The conversion range of the ADC can be specified to produce a low LSB, so the resolution of the readout circuit can be increased. This can be achieved by setting the positive reference voltage, `VRP` and negative reference voltage, `VRN` of the ADC into both upper and lower limit of the output range which are presented in Table 4.2. The LSB of the ADC can be obtained by

$$LSB = \frac{VRP - VRN}{1024} = \frac{2.65 - 1.525}{1024} = 0.8584mV \tag{4.3}$$

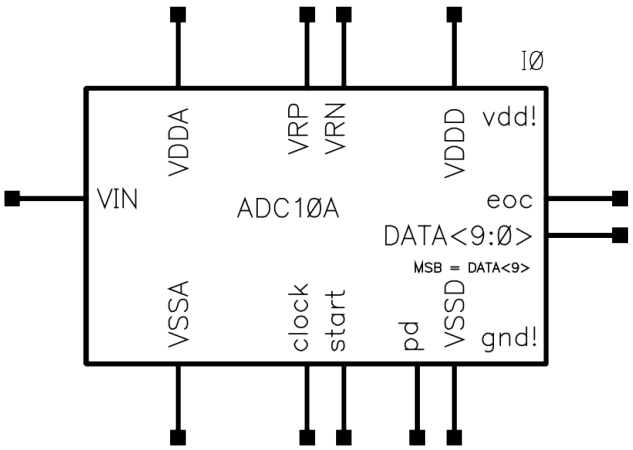


Figure 4.9 CMOS 10-Bit ADC

Current Direction	VRP	VRN
Into WE	2.65	1.775
Out from WE	0.65	1.525

Table 4.2 Reference voltage setup in ADC for bidirectional current

The input current can thus be determined from the decimated output of the ADC.

4.6 Operation Mode Settings

As mentioned in section 4.1, the wide dynamic range of the input current is achieved by varying the integration frequency and capacitance. Firstly, the highest integration frequency should be determined. Based on the datasheet of the ADC, the clock frequency of the ADC is 1.1 MHz and it takes 11 clock cycles to complete a single conversion. Thus, the maximum integration frequency that can be used is 100 kHz. The frequency is divided by 8 in the subsequent mode to ease the implementation of the digital part of the circuit at the later stage. Different capacitor is also used to further expand the dynamic range of the input current. The capacitor values are chosen carefully to avoid a large die size. The different mode settings with their respective integration frequency and capacitor are presented in Table 4.3. The lower mode is limited by the minimum capacitance of the AMS410 c35b4 technology which is 89.44 fF and long integration time. The higher mode could be implemented by increasing capacitor size. However, it is not done in this project since the input current from the working electrode is usually less than 20 μA and other challenges like power consumption due to high output current, and large die size due to large capacitor size might arise as well.

The input current range presented in Table 4.3 is only the current which gives less than 1% deviation. The current range is actually wider than that. However, the circuit can measure current within $\pm$ **13 μA** with the minimum input-referred noise of 44 fF. The methods of calculation for minimum

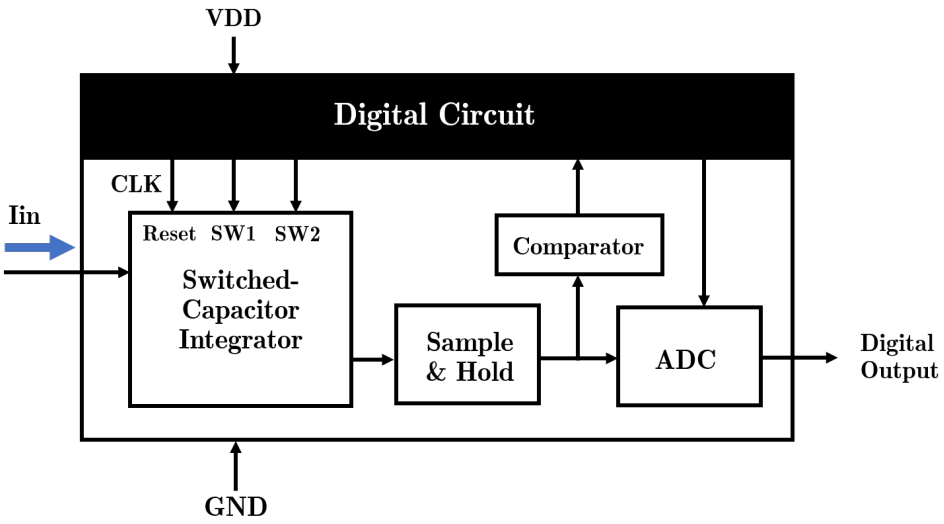


Figure 4.10 Analogue block diagram of the readout circuit where the black box represents the digital circuit for autonomous gain control which will be explained in the next chapter

Mode	Input Current	Integration Time	Capacitor
0	1 - 8 μA	5 μs	40 pF
1	0.125 - 1 μA	5 μs	5 pF
2	15.63 - 125 nA	40 μs	5 pF
3	1.95 - 15.63 nA	320 μs	5 pF
4	0.24 - 1.95 nA	2.56 ms	5 pF
5	30.52 - 244.14 pA	20.48 ms	5 pF
6	3.82 - 30.52 pA	20.48 ms	625 fF
7	0.47 - 3.82 pA	163.84 ms	625 fF

Table 4.3 Different mode settings

input-referred noise will be explained later.

4.7 Circuit Level Simulation

The analogue circuit is tested by using parametric simulation in which the working electrode is modelled using a resistor. Different modes are tested to determine its dynamic range and noise.

4.7.1 Dynamic Range

As mentioned in the previous chapter, the two main sources of the error for the switched-capacitor integrator [14] are

1. the **finite transconductance**, G_m of the folded cascode transconductance amplifier
2. the **on-resistance**, r_{on} of the low leakage switch

Referring back to equation 4.4, to keep the error as low as possible, both r_{on} and G_m values need to be adjusted carefully in order to cancel out each other and thus minimise the total offset.

$$\frac{V_{out}}{I_{in}} = \frac{1}{2f_{clk}C_{int}} + r_{on} - \frac{1}{G_m} \tag{4.4}$$

For this switched-capacitor topology, the dynamic range of the input current with less than 1 % deviation is from 0.47 pA to 8 μA. This parameter has improved significantly compared to the switched-capacitor integrator designed in Chapter 3. A graph of output voltage against input current for different mode settings is presented in Fig. 4.11.

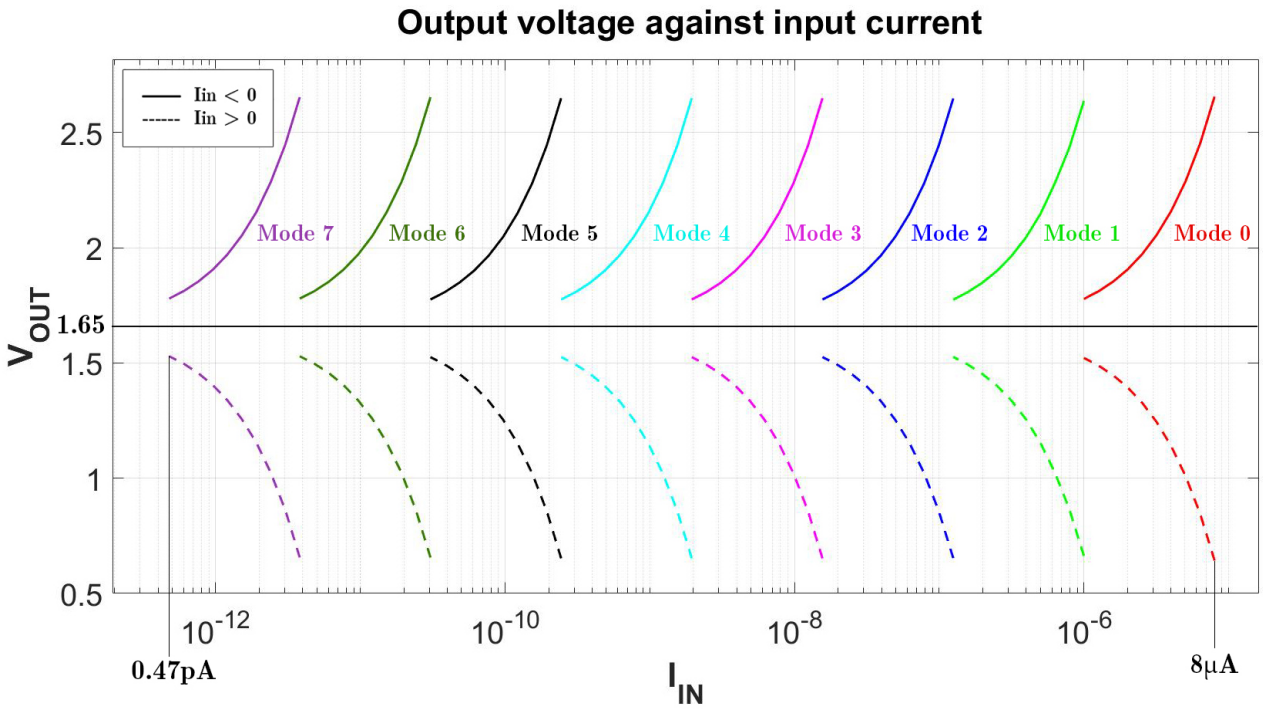


Figure 4.11 Output voltage against input current for different mode settings

4.7.2 Noise

The total input-referred current noise ${I_{in}}^2$ is the minimum detectable current of the switched-capacitor integrator [21]. It needs to be determined for each operating mode. To compute ${I_{in}}^2$, the total output voltage noise, ${V_{out}}^2$ at the sample and hold node is required. This can be done by running periodic steady state analysis (PSS). PSS analysis is carried out to compute the periodic operating point when the circuits are linearised around a periodic steady state operating point. Then, the operating point will be used in subsequent phase noise (Pnoise) analysis. The settings for both analysis is displayed in Table 4.4. Shooting method is chosen for PSS analysis since it can reduce the computational time significantly. The maximum sideband parameter is used in pnoise analysis to determine how much of aliasing should be considered. The default value of 7 is chosen. This is because the simulations will run unnecessarily long if the value is too large or the noise will be underestimated if the value is too small.

Parameter	Setting
Beat Frequency	f_{clk}
Engine	Shooting
Maximum sideband	7

Table 4.4 PSS and Pnoise analysis settings

The total output noise is then calculated by integrating the phase noise graph over the -10 dB bandwidth, f_{-10dB}, which is the noise bandwidth. Next, the relationship between ${I_{in}}^2$ and ${V_{out}}^2$ is drawn to work out ${I_{in}}^2$.

$$V_{out} = \frac{1}{C_{int}} \int_0^{\frac{T_{clk}}{2}} I_{in} dt \tag{4.5}$$

$$V_{out} = \frac{T_{clk} I_{in}}{2C_{int}} \tag{4.6}$$

$${I_{in}}^2 = (2C_{int} f_{clk})^2 {V_{out}}^2 \tag{4.7}$$

The input-referred noise for each mode is presented in Table 4.5. The circuit has a minimum input-referred noise as low as 44 fA at the highest mode.

Mode	Input Current	Output Noise (V^2/Hz)	f_{-10dB}	Input-Referred Noise, I_{in}^2
0	1 - 8 μA	63.1 n	68 k	524.3 nA
1	0.125 - 1 μA	68.6 n	76 k	72.2 nA
2	15.625 - 125 nA	37.6 n	9.25 k	2.3 nA
3	1.953 - 15.625 nA	8.4 n	3.17 k	802 pA
4	0.244 - 1.953 nA	2.1 n	2.09 k	32 pA
5	30.52 - 244.14 pA	0.46 n	138.74	6.2 pA
6	3.815 - 30.52 pA	0.92 n	160.43	117 fA
7	0.477 - 3.815 pA	0.59 n	22.49	44 fA

Table 4.5 Output noise and input-referred current noise for different mode settings

4.8 Chapter Summary

In this chapter, each part of the switched-capacitor readout circuit is explained in detail. The readout circuit operation is broken down into different operating mode, each for different ranges of input current, thus expanding the input dynamic range of the readout circuit. Different mode settings are achieved by manipulating the integration frequency and capacitance. The switched-capacitor topology shows a significant improvement in terms of dynamic range compared to the circuit designed in Chapter 3. Hence, the switched-capacitor topology is chosen as the analogue readout circuit. Lastly, different operating modes with their respective input-referred noise are presented. However, the readout circuit still requires manual tuning of the frequency and activation of the switches for the capacitors. This leads to the implementation of the digital circuit for autonomous gain control in the next chapter.

Chapter 5

Digital Circuit

The circuit described in Chapter 4 is able to detect a wide dynamic range of input current. However, the frequency and capacitance need to be changed accordingly to provide a linear measurement. To ease the tuning process, an autonomous gain control algorithm is implemented to vary the mode of the switched-capacitor based on the input current. A mealy state diagram for the autonomous gain control algorithm is presented in Fig. 5.1 and its operation is explained in detail in the following sections. Each arrow represents the conditions that have to be satisfied in order to transition to the other state.

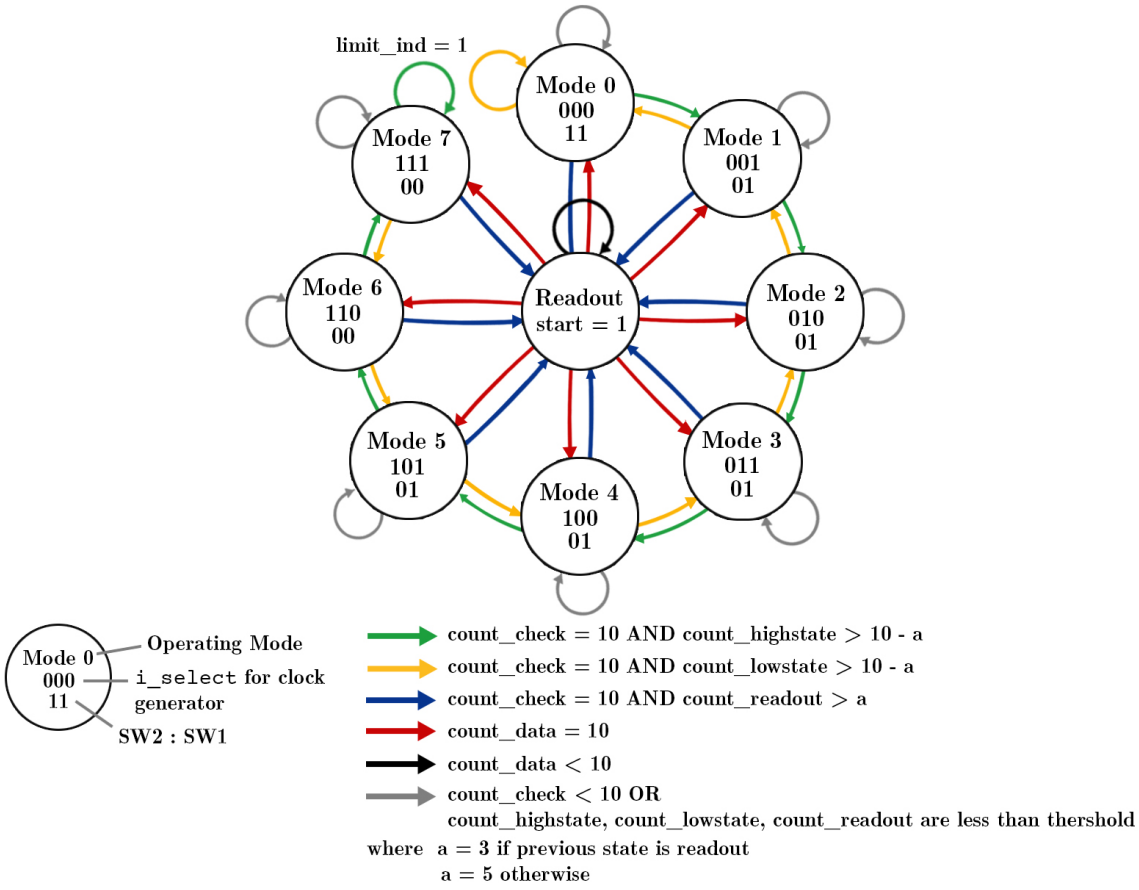


Figure 5.1 Mealy state diagram for AGC

5.1 Clock Generator

As mentioned in the previous chapter, different integration frequencies are required for different mode operations. Hence, a clock generator which is capable of generating all the local clocks with the required frequencies from the 100 kHz system clock is needed. Since each local clock frequency is a multiple of 1/8 of the system clock frequency, the design process is very simple and straightforward as shown in Listing 5.1.

```
with i_select select
  o_clk_div <=  i_clk              when "000", --Mode 0: f= 100kHz, Tint= 5us
                i_clk              when "001", --Mode 1: f= 100kHz, Tint= 5us
                clk_divider(2)     when "010", --Mode 2: f= 12.5kHz, Tint= 40us
                clk_divider(5)     when "011", --Mode 3: f= 1562Hz, Tint= 320us
                clk_divider(8)     when "100", --Mode 4: f= 195Hz, Tint= 2.56ms
                clk_divider(11)    when "101", --Mode 5: f= 24Hz, Tint= 20.48ms
                clk_divider(11)    when "110", --Mode 6: f= 24Hz, Tint= 20.48ms
                clk_divider(14)    when "111", --Mode 7: f= 3Hz, Tint= 163.84ms
                i_clk              when others; --To initialise the clock
```

Listing 5.1 Code snippet of clock generator

`clk_divider` is a counter which is added by 1 at each rising edge of the system clock. The LSB of the `clk_divider` then has a frequency which is half of the frequency of the system clock. Bit 2 of `clk_divider` is thus corresponds to a clock signal with 1/8 of the system clock. The rest of the frequencies correspond to higher bits of `clk_divider`. To reduce power consumption, `when` statements are used so the clock generator only outputs the required frequency based on the bit pattern of `i_select`.

5.1.1 Clock Optimisation

Although the operation of the clock generator seems fine, the following problems are noticed after a few simulations are carried out.

1. The system clock frequency is set at 100 kHz initially to account for 5 μs integration time. However, this system clock cannot be used to drive the ADC as it will slow down the conversion as the maximum clock frequency of the ADC is 1 MHz.

2. Data acquisition time is long due to long hold time especially in higher mode. This is because the duty cycle of each clock frequency is set at 50 %, long integration time implies long hold time as well.

Long hold time is pointless since the comparator can compare the output voltage with the reference voltage directly after integration. Thus, the hold time can be reduced but the integration time is kept the same as the previous design. Hence, the speed of the readout circuit can be improved significantly. The time for a single conversion in ADC needs to be taken into consideration in deciding the hold time as well. Based on the datasheet of the ADC, the ADC conversion is completed after 11 clock cycles,

thus 12 μs is set to be the hold time. The system clock frequency is changed to **1 MHz** to drive both the clock generator and ADC at the same time.

The clock generator now uses a counter, called `counthigh`, which counts up by one at each rising clock edge of the system clock. For the highest frequency mode, the output clock, `o_clk_div`, stays high for 5 clock cycle to set 5 μs of integration time, followed by another counter, called `countlow` which set the hold time by staying low for another 12 μs to allow ADC conversion. Similarly, for the lowest frequency mode, the output clock stays high for 163840 clock cycles and then low for 12 clock cycles. The improvement is obvious especially in low frequency mode since the hold time is 12 clock cycles instead of 163840.

```
    case current_state is
    when statehigh =>
      if(counthigh < cycle_no - 1) then
        o_clk_out <= '1';
      else
        o_clk_out <= '1';
        current_state <= statelow;
        countlow <= 0;
      end if;
      counthigh <= counthigh + 1;

    when statelow =>
      if(countlow < 11) then
        o_clk_out <= '0';
        countlow <= countlow + 1;
      else
        o_clk_out <= '0';
        current_state <= statehigh;
        counthigh <= 0;
      end if;

    end case;
```

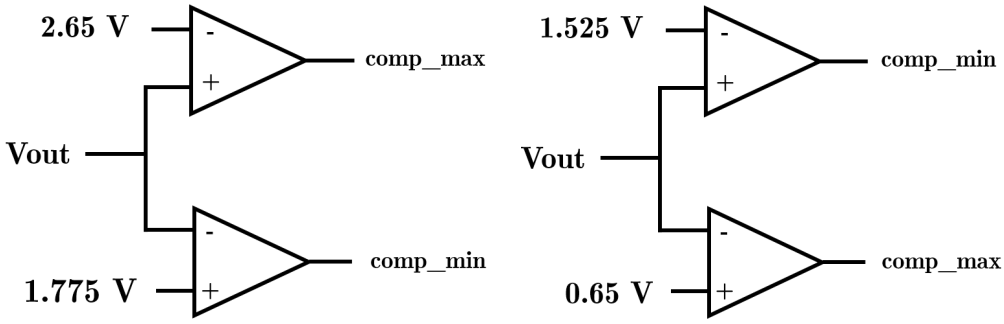
Listing 5.2 Code snippet of improved clock generator

5.2 Autonomous Gain Control Algorithm

Since each mode yields an output voltage range with respect to their input current range, thus the upper and lower limit of the voltage can be used as a threshold to determine if the circuit should operate at higher or lower mode, or stay at the same current mode. The algorithm of the autonomous gain is explained in detail in the following subsections.

5.2.1 Mode Specification Stage

Firstly, the output voltage from the sample and hold, V_{out} is transfered to the two clocked comparators designed in Chapter 4. The comparators are named **comp_max** and **comp_min** respectively. The comp_max comparator compares the output voltage with a reference voltage which is the upper limit of the voltage range, while the comp_min comparator compares the output voltage with a reference voltage which is the lower limit of the voltage range.



(a) Current into WE (b) Current from WE

Figure 5.2 The comparator pair setup for bidirectional current

When both comparators go low, it indicates the voltage is well within the output range, thus it should stay in the current mode. If comp_max goes high while the comp_min goes low, this indicates the output voltage is higher than the upper limit. In other words, the current is too large. Hence, the integrator needs to shift to a lower state which is capable of measuring larger current. If the comp_max goes low while the comp_min goes high, this indicates the output voltage is lower than the lower limit and the input current is too small. Hence, the integrator needs to shift to a higher state to measure small currents. The operation is summarised in Table 5.1.

comp_max	**comp_min**	**Operation**
Low	Low	Stay at current mode
High	Low	Shift to lower mode
Low	High	Shift to higher mode

Table 5.1 The operation of the comparator pairs

5.2.2 Mode Specification Optimisation

Although the algorithm for mode specification seems sufficient, it is yet to be true; the reason being that it does not consider variations at the input current that are likely to happen. For example, if the measurement takes place when there is a momentary variation at the input current, then the measured current could be big enough to provide a high comp_max output at the digital block. This is undesirable

as it will lead to a shift to lower mode.

In order to compensate the momentary variation of the input current, the operation of the digital block is expanded. The circuit only changes its mode (i) after N measurements are taken and (ii) if the results from N measurements exceed the threshold values, α and β. The relationship between N, α and β are given by:

$$N = \alpha + \beta \tag{5.1}$$

where N is the number of measurements taken, α is the threshold for readout stage and β is the threshold for changing mode. N is set at 10 to take 10 measurements for decision-making of the next stage. 10 is a fairly good sample size assuming the momentary variations of the current is less than five clock cycles during the mode specification stage. α and β are set to 5 which is half of the sample size, N.

More specifically, the digital block needs to receive 10 comparator pair outputs measured at the same mode. The mode will only change if more than **five** of them indicate that the mode needs to be changed. Three counters, **`count_readout`**, **`count_highstate`** and **`count_lowstate`** are declared to store the results of each comparator pair output from each rising clock edge. For example, if 6 out of the 10 comparator outputs indicate the current is at the correct operating mode, `count_readout` will count up to 6 and the circuit will shift to readout mode with the same mode settings at the next clock phase since **`count_readout`** $> \alpha$. If 6 of the 10 comparator outputs indicates change to lower mode is required, `count_lowstate` will count up to 6 and the circuit will shift to a lower operating mode in the next clock phase since **`count_lowstate`** $> \beta$. The same goes to `count_highstate`. If none of the conditions are satisfied, the circuit will stay in the same mode in the next clock phase. An example of the operation of the counters is summarised in Table 5.2. The code snippet of this operation is shown in Listing 5.3.

`count_readout`	**`count_highsate`**	**`count_lowstate`**	**Result**
6 ($> \alpha$)	2	2	Shift to readout stage
1	7 ($> \beta$)	2	Shift to higher mode
1	1	8 ($> \beta$)	Shift to lower mode
5	3	2	Stay at current mode

Remark:
`count_readout` indicates the output is within the range
`count_highsate` indicates the output is lower than the range
`count_lowstate` indicates the output is higher than the range

Table 5.2 An example of the operation of counters

```
when s1 =>
    sw1 <= '1';        --switch setting for Mode 1
    sw2 <= '0';
    frequency <= "000";    --frequency setting for Mode 1

    if(count_check = 10) then --check the counter after getting 10 comp outputs
        if (count_readout > 6) then
          current_s <= readout; --chenge to readout stage
        elsif (count_highstate > 6) then
          current_s <= s2; --change to higher mode
        elsif (count_lowstate > 6) then
          current_s <= s0; --change to lower mode
                else
                  current_s <= s1; -- stay at current mode
        end if;
```

Listing 5.3 Code snippet of the counter operation at Mode 1

In extreme cases where the input current is beyond the limit of the measurement of the switched-capacitor integrator, the **limit_ind** signal of the digital block will be high to indicate the readout circuit has reached its limit and unable to measure the current. For example, if the input current is very large, the circuit will stay at the lowest operating mode and `limit_ind` will be high.

5.2.3 Readout Stage

After mode specification stage where the circuit has changed to the correct operating mode with respect to the input current, the circuit will shift to the readout stage where the output voltage is passed to ADC. After taking 10 data, the circuit should shift back to previous mode of the mode specification stage since the input current will most likely at the same decade. Based the description of the algorithm, it can be seen that the ADC is not used at the mode specification stage. Turning on the ADC only at the readout stage will lead to a significant reduction in power consumption of system. The reason for that is that the ADC is a power intensive block which consumes significant amount of power if operates continuously. In order to turn on the ADC, an extra **start** signal which is usually low is declared in the digital block. The signal is only high at the readout stage to start the ADC.

```
    when readout =>
      if (count_data < 10) then --check if 10 data are collected
        start <= '1'; --start the ADC
        count_data <= count_data + 1;
        current_s <= readout; --collect next data
      else
        current_s <= previous_s; --return to the previous stage
        count_data <= 0; --reset the counter
      end if;
```

Listing 5.4 Code snippet of the readout stage

5.2.4 Hysteresis Operation

To further improve the stability of the readout circuit, hysteresis operation is added into the digital block operation. This modification can ensure the circuit does not oscillate between different states without entering the readout stage. The hysteresis operation can be done by altering both threshold values, α and β. For example, if the previous state is readout stage, then current mode is most likely the correct mode for the input current assuming there is no significant changes in decades in the input current. α is then changed to 3 while β is changed to 7. The value of 3 is chosen to make the circuit more difficult to change its mode. Hence, the circuit will tend to stay in the same mode and then shift to readout state to read the data unless the change in input current is large and long enough to trigger changes in mode. α and β values will reset to 5 if the previous stage is not readout. Table 5.3 summarises the threshold values for hysteresis operation.

Parameter	**Without** Hysteresis	**With** Hysteresis
α	5	3
β	5	7
N	10	10

Table 5.3 The threshold values for different conditions

```
if (previous_s = current_s) then
      threshold := 3; --change the threshold if previous stage is readout
    else
      threshold := 5; -- typical threshold
    end if;

    case current_s is
    when s0 =>

      sw1 <= '1';
      sw2 <= '1';
      frequency <= "000";

      if(count_check = 10) then
        if (count_readout > threshold) then -- threshold for readout
          current_s <= readout;
        elsif (count_highstate > 10-threshold) then -- threshold for mode change
          current_s <= s1;
        elsif (count_lowstate > 10-threshold) then
          limit_ind <= '1'; -- limit indicator
          current_s <= s0;
        end if;
```

Listing 5.5 Code snippet of the hysteresis operation

In a nutshell, the addition of hysteresis operation makes the overall system more stable and tends to stay at the current mode for readout. Thus more data can be collected during readout instead out keep on changing mode due to the effects of noise. The values of N, α and β could be designed in such a way that they can be varied based on the nature of the analytes and the sensing environment to further improve the hysteresis.

5.3 RTL Simulation

The description language chosen for the design of the digital block is VHDL. The VHDL is chosen because it can be used across all programmable logic and ASIC technologies and thus allow design migration path. It is also a standard and supported by all major tools vendor. Most importantly, VHDL is a strongly-typed language. As a result, designs written in VHDL are considered self-documenting and ease the debugging process [22]. The complete codes were developed and shown in the Appendix.

5.3.1 Clock Generator

The VHDL code for the clock generator called **`freq_select`** is imported and its symbol is generated as shown in Fig. 5.3. It consists of three inputs and an output clock. RTL simulation is then carried out using ModelSim simulator to test the behaviour of the digital block. The result of the simulation for the clock generator is shown in Fig. 5.4. Based on the result, the frequency generator operates as expected and generates clock signal with the correct frequency based on the bits of the `i_select`. For example, when `i_select` is 000, the generator outputs a clock signal which stays high for 5 system clock cycles and low for 12 system clock cycles. When `i_select` is 010, the clock signal stays high for 40 cycles.

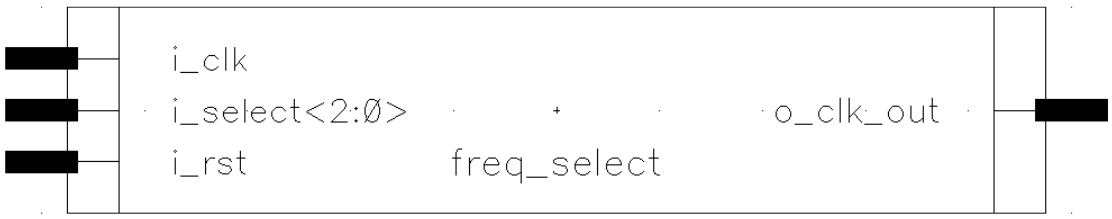


Figure 5.3 Symbol of clock generator.

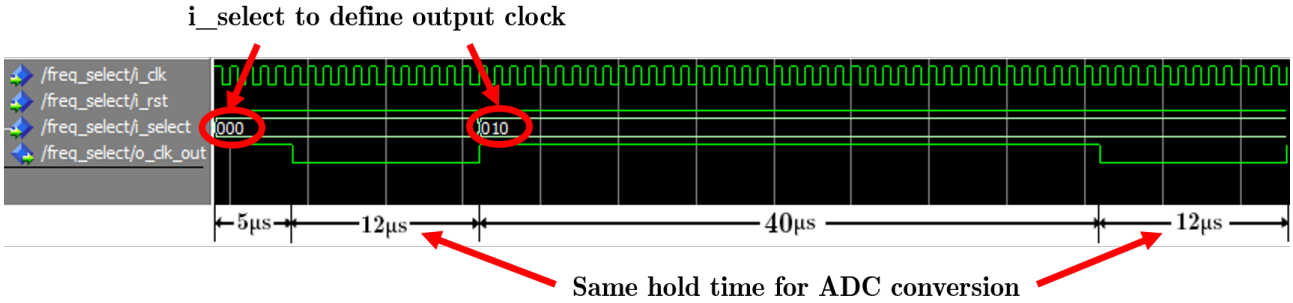


Figure 5.4 RTL simulation for clock generator.

5.3.2 Autonomous Gain Control

The autonomous gain control algorithm is also tested using ModelSim simulator. The VHDL code for the autonomous gain control is imported and the symbol generated is shown in 5.5. The state for the operation begins at Mode 0 and then transitions to other states depending on the number of each counter after ten clock cycles. Fig. 5.6 shows the state changes from `S0` to `readout` stage. After 10 counts by `count_check`, `count_readout` has exceeded the threshold which is 5 in this case, then the state changes to `readout`. During readout stage, `start` signal stays high to initiate the ADC and `count_data` begins to count the data collected. After 10 data have collected, the state returns to `S0` again.

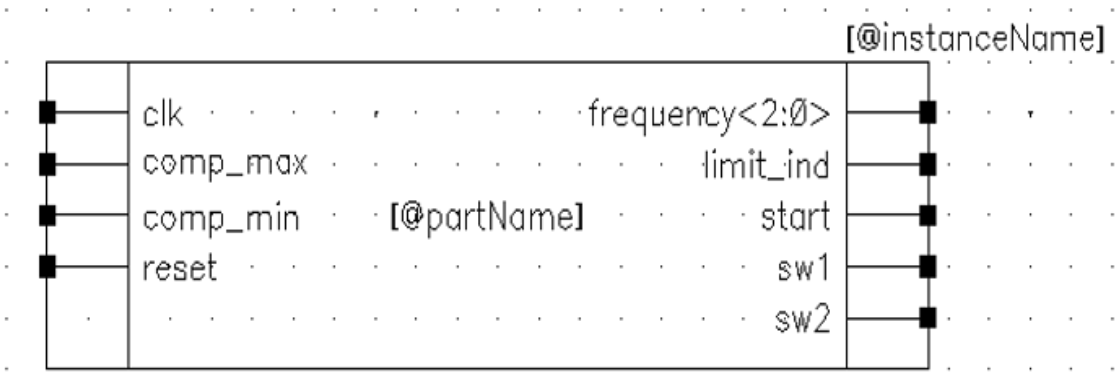


Figure 5.5 Symbol of autonomous gain control circuit

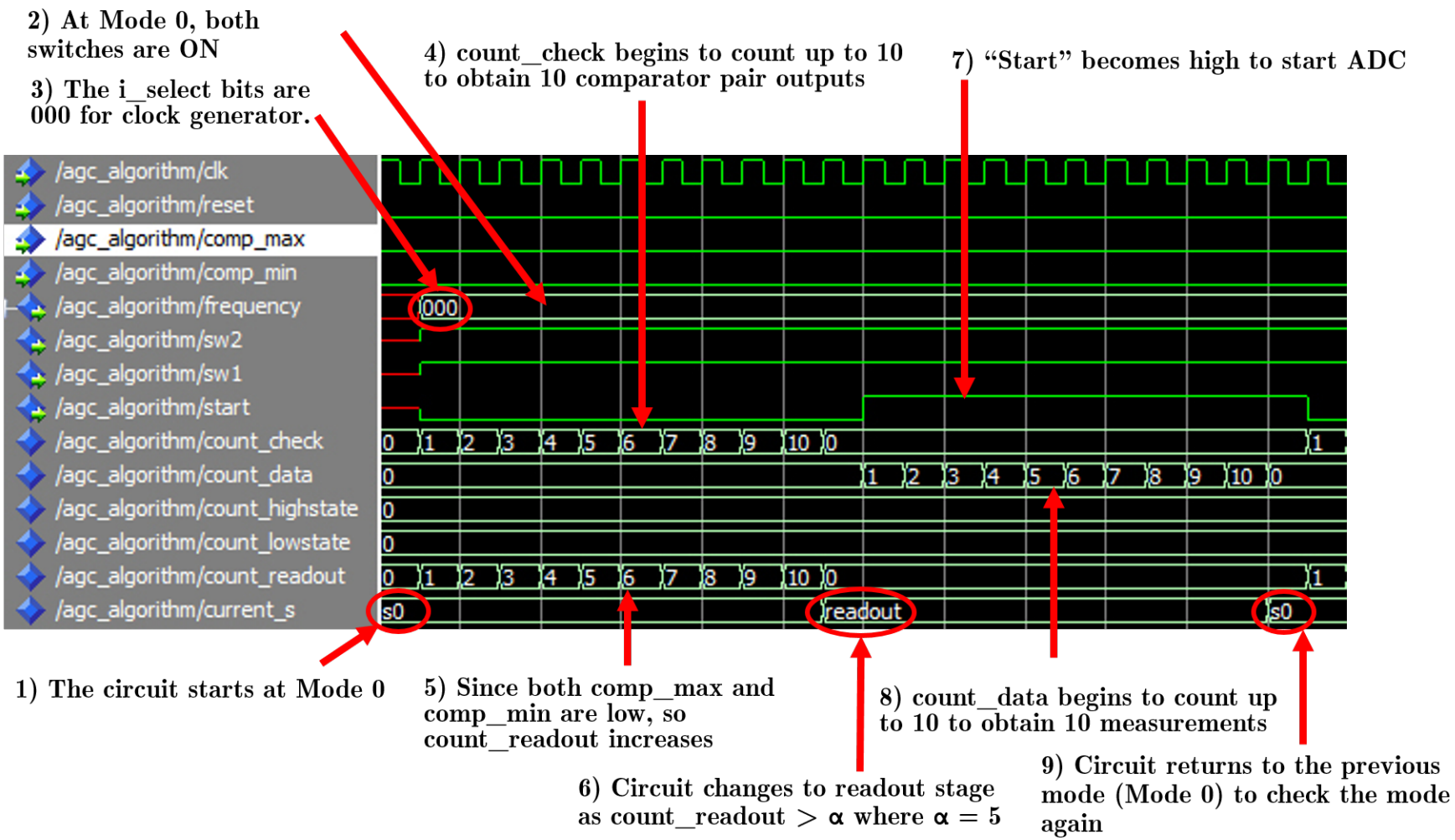


Figure 5.6 RTL simulation shows the transition to the readout stage by following steps 1 to 9

The hysteresis operation can be observed when the state is returned from the readout stage where the threshold has changed to 3. Thus the digital circuit will transition to `readout` stage as long as `count_readout` is more than 3 as shown in Fig. 5.7.

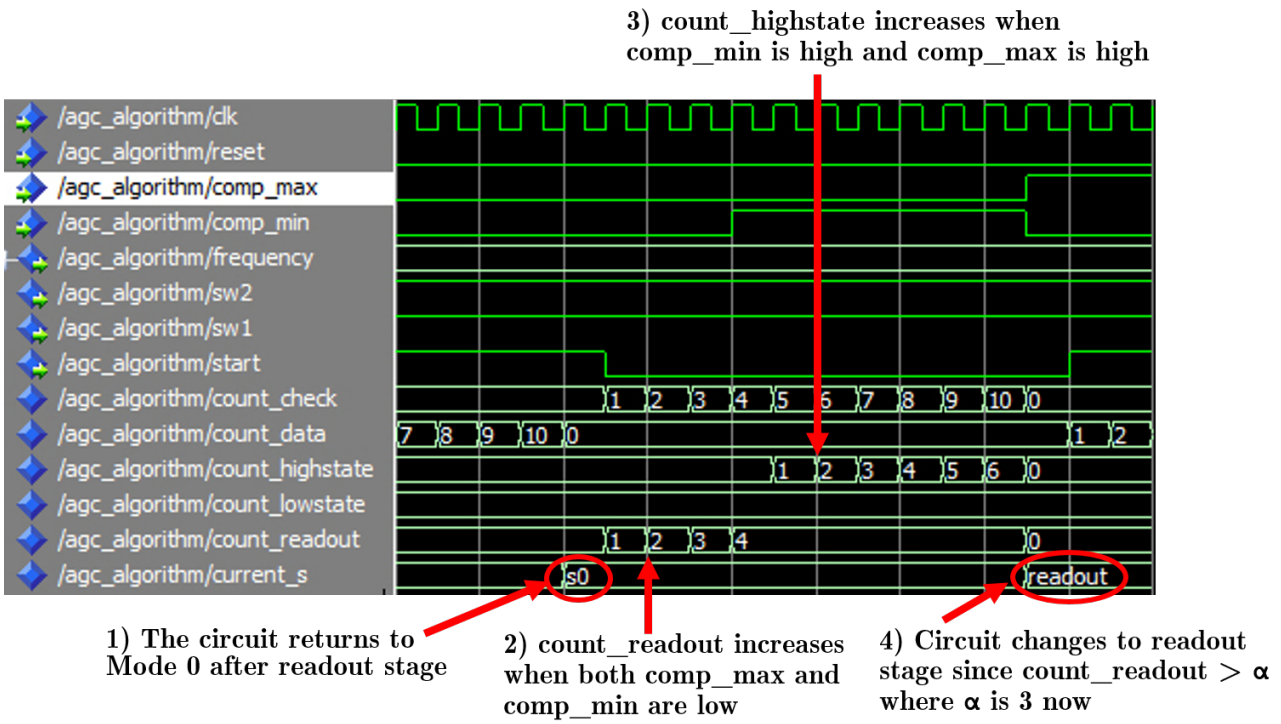


Figure 5.7 RTL simulation continued from Fig. 5.6. The hysteresis operation is shown by following steps 1 to 4.

5.4 Chapter Summary

Chapter 5 describes two main blocks of the digital circuits, the clock generator and autonomous gain control circuit. The operation principles and the algorithm of the VHDL codes are explained in detail. The additional features such as hysteresis and power saving modifications were made to improve its performance. A mealy state diagram is also drawn to summarise the operation of the autonomous gain control algorithm. RTL simulations for each digital block are carried out and presented at the end of the chapter. The whole system which consists of both analogue and digital circuits are simulated in the next chapter.

Chapter 6

System Level Simulation

The overall system block diagram combining both analogue and digital blocks is presented in Fig. 6.1. System level simulations are carried out to verify the overall performance of the readout circuit. The simulation results are presented in the following sections. The two stages of the system is also illustrated in Fig. 6.2.

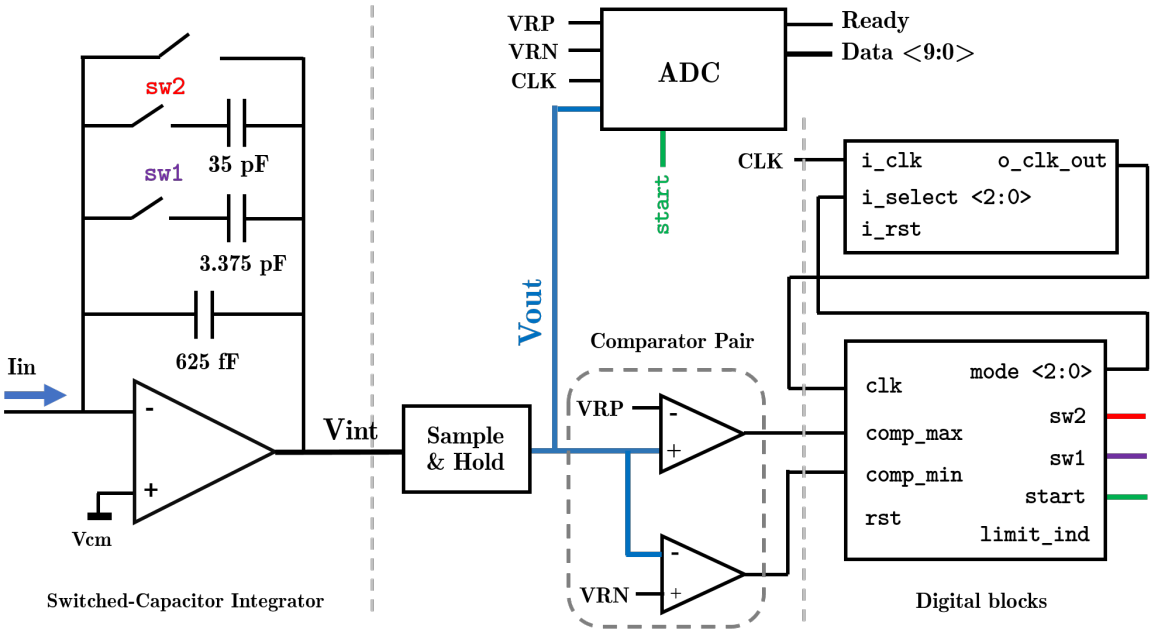


Figure 6.1 Readout circuit system block diagram

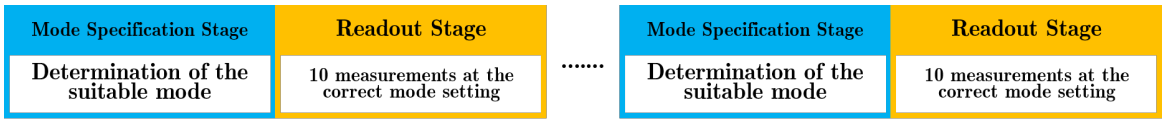


Figure 6.2 The two stages of the digital block

6.1 Transient Simulation

In transient simulation, different input currents are applied to the readout circuit to model the behavior and test the performance of the readout circuit. Due to the extremely long simulation time of AMS simulation, most of the transient simulations in this section are performed at lower modes.

6.1.1 Constant Input Current

The system is first tested with a constant input current to observe the mode specification stage and readout stage. In this simulation, an input current of 62.5 nA is transferred into the system. As seen in Fig. 6.3, the readout circuit begins to integrate the input current at Mode 0 settings. However, the integrated voltage is not large enough to provide detectable a measurement. The circuit then changes to Mode 1 where a smaller integration capacitor is used but the integrated voltage is still small. At Mode 2, the integration time is then increased. Hence, the output voltage is now within the voltage range, thus the digital circuit generates a high `start` signal to initiate the readout stage. The output voltage is converted into 10-bits digital output and 10 data are collected during readout stage. As shown in Fig. 6.3, all the ADC outputs are 0110110111 in hex, or 439 in decimal.

To determine the input current from the ADC output, the integrated voltage needs to be determined first. This can be done by reverse calculation:

$$V_{out} = VRN + 439 \times 1LSB \tag{6.1}$$
$$V_{out} = 1.775 + 439(0.8545m) \tag{6.2}$$
$$V_{out} = 2.15 \tag{6.3}$$

Given the integrating capacitor and time for Mode 1 is 5 pF and 40 μs respectively, the input current can therefore be determined. The calculated input current is corresponding to the input current applied at the readout circuit.

$$I_{in} = \frac{C_{int}(V_{out} - V_{cm})}{t_{int}} \tag{6.4}$$
$$I_{in} = \frac{5 \times 10^{-12} \times (2.15 - 1.65)}{40 \times 10^{-6}} \tag{6.5}$$
$$I_{in} = 62.5nA \tag{6.6}$$

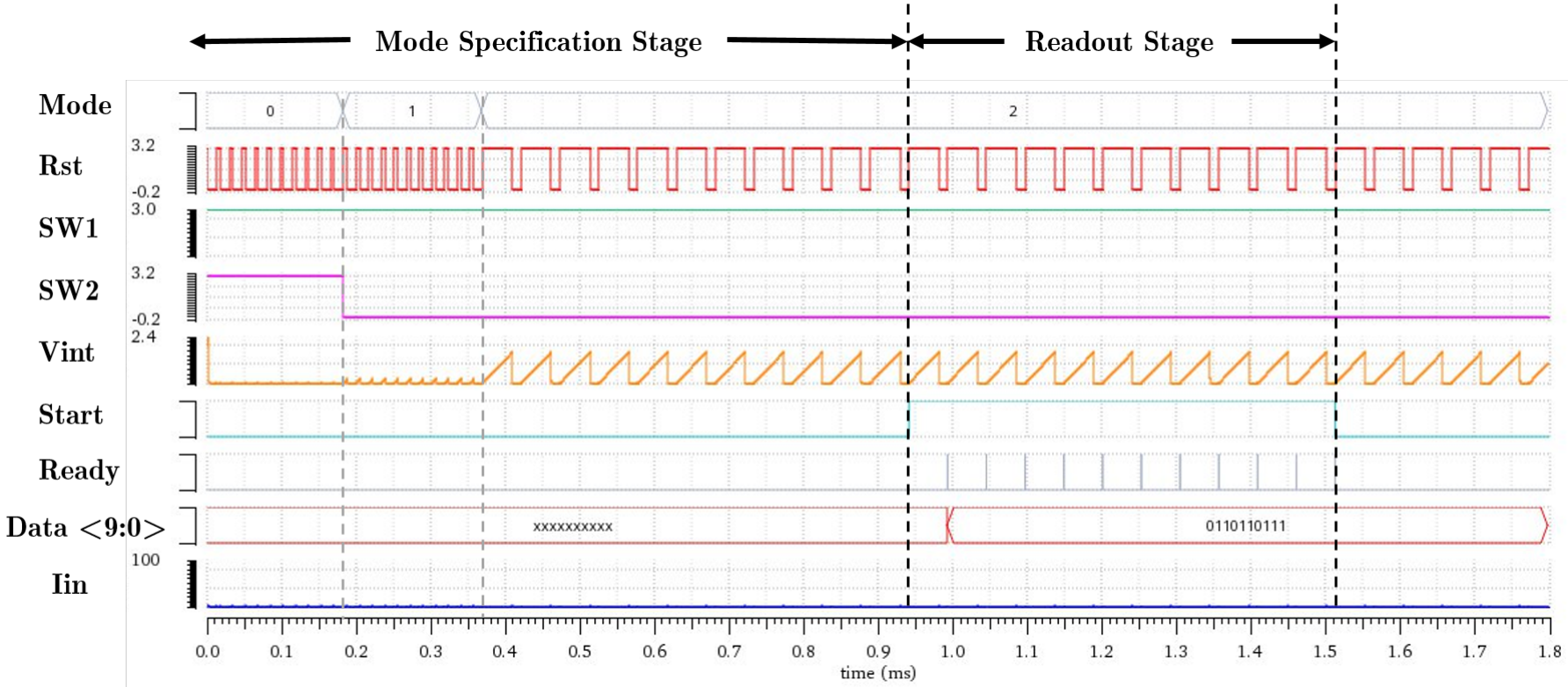


Figure 6.3 Readout circuit operation for a constant input current. At Mode 0, both switches are closed. However, the current is too small to generate a significant output voltage. The circuit then changes its operating mode at Mode 1 where SW1 is opened but the output voltage is still small. At Mode 2 where the integration time has increased, the output voltage is well-within the range. Lastly, the circuits begin to start ADC to take measurements in readout stage and return to Mode 2 again.

6.1.2 Noisy Input Current

Although the readout circuit is able to generate an accurate output based on the simulation and calculation in the previous section, however this is not a good justification on the performance of the readout circuit. In the real sensing environment, there will be a lot of noise in the sensor current from the working electrode due to the electrode-analyte interface, concentration of analyte [23], electrode asymmetry [24] or interferences from other electro-active molecules in the solution or the presene of nano-structures [25].

To model such signal, current with momentary spikes and variations is generated using `vpwl`. The simulation setup is shown in Fig. 6.4. The spikes generated are large and span across wide range in short time. This signal is then transferred to the readout circuit to determine if the system is capable of detecting the current accurately.

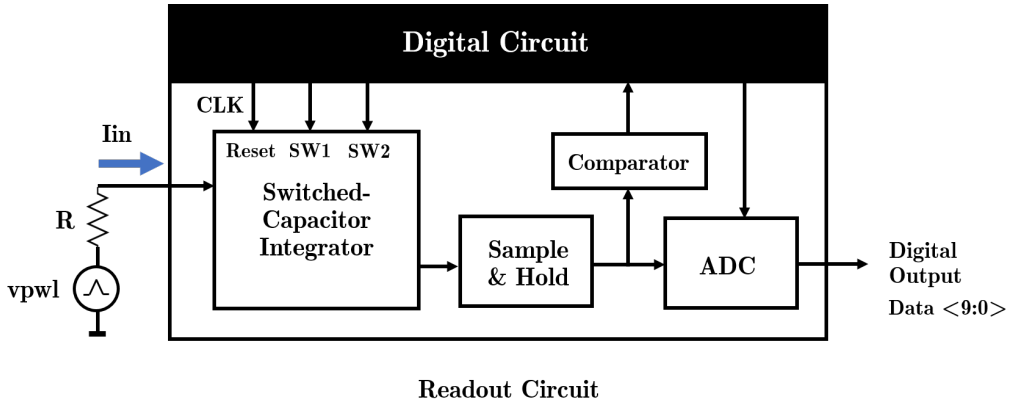


Figure 6.4 Simulation setup for noisy input current simulation.

Owing to the 10 measurements taken during the mode specification stage, the system managed to transition to an appropriate mode. However, the noise in the input signal does affect some of the ADC outputs collected during the readout stage. This is because the momentary current spikes are integrated at the capacitor as well. By taking the average of the 10 ADC outputs, the input current obtained is **61.3 nA**. There is an offset in voltage source due to the spike. This offset is calculated and gives an average of 3.3374 V. Thus, the average input current generated due to the noisy source is approximately **61.1 nA** which is very close to the current calculated from ADC output.

To rectify the noise problem, differential sensing by using a second WE [26, 27] to sense the background current and then subtract it from the main WE to obtain a noiseless differential input. This technique is suitable for glucose and lactate with gradually changing concentration. For metabolites like dopamine with rapid changing, technique like sensing the background current in the absence of the biomolecules and then performing subtraction from the sensor current [28] can be adopted.

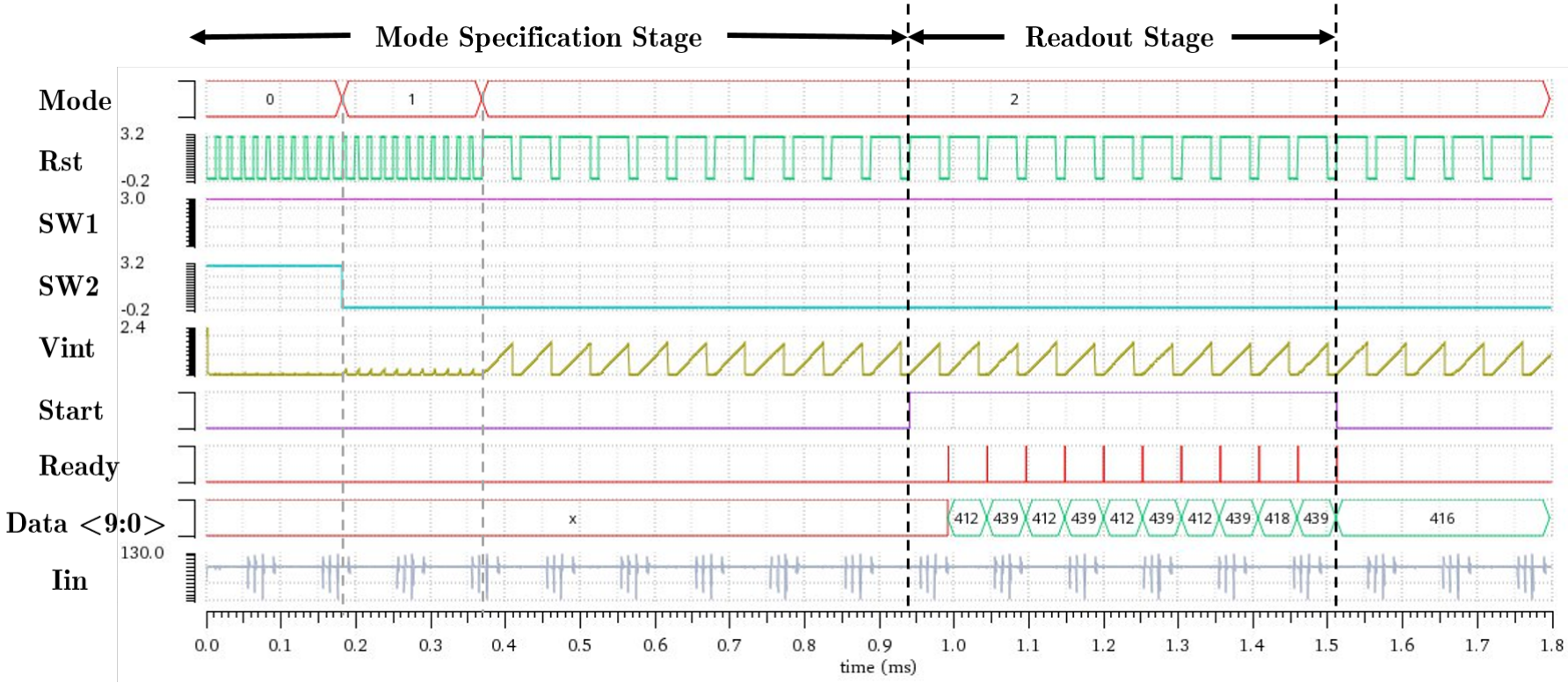


Figure 6.5 Readout circuit operation for an input current with noise. In the presence of noise, the readout circuit still managed to transition to a suitable mode. However, the ADC output is affected.

6.1.3 Varying Input Current

In the real sensing environment, the current from the WE is always changing due to the changes in concentration of analytes in biochemical events. To characterise how fast the system responds to a change in current, an input current with sudden change is applied to the system. Fig. 6.6 illustrates how the system responds to an input current with sudden changes from **250 nA to 45.54 nA**. The changes span over a decade and thus a change in mode is expected.

At the beginning, a current of 250 nA flows into the WE and causes the discharge of the integrating capacitor. This current is too small for Mode 0 to produce detectable output voltage changes. Hence, the circuit transitions to Mode 1 where the integrating capacitor becomes smaller. Initially, during the first three clock cycles, the current is sufficient to produce an output voltage which is within the range but there is a sudden change of current to 45.54 nA. Hence, Mode 1 is now not suitable for measuring this current. Owing to the threshold value set, the circuit then changes to Mode 2 despite there are 3 values which indicate the system should stay in Mode 1. At Mode 2, the circuit then performs readout by starting the ADC conversion. The output of the ADC is -278 in decimal. Since the VRN for current flowing into WE is 1.525V, the current can be determined by:

$$V_{out} = 1.525 - 278(0.8545m) = 1.287V \tag{6.7}$$

$$I_{in} = \frac{5 \times 10^{-12} \times (1.65 - 1.287)}{40 \times 10^{-6}} \tag{6.8}$$

$$I_{in} = 45.4nA \tag{6.9}$$

After the readout stage at Mode 2, the current changes back to 250 nA. The integrating capacitor now discharges rapidly and output voltage is below the lower limit of the voltage range. After mode specification stage, the system transitions back to Mode 1 and then begins the readout stage. The output of the ADC is -144 which corresponds to 250 nA of input current.

$$V_{out} = 1.525 - 144(0.8545m) = 1.4V \tag{6.10}$$

$$I_{in} = \frac{5 \times 10^{-12} \times (1.65 - 1.4)}{5 \times 10^{-6}} \tag{6.11}$$

$$I_{in} = 250nA \tag{6.12}$$

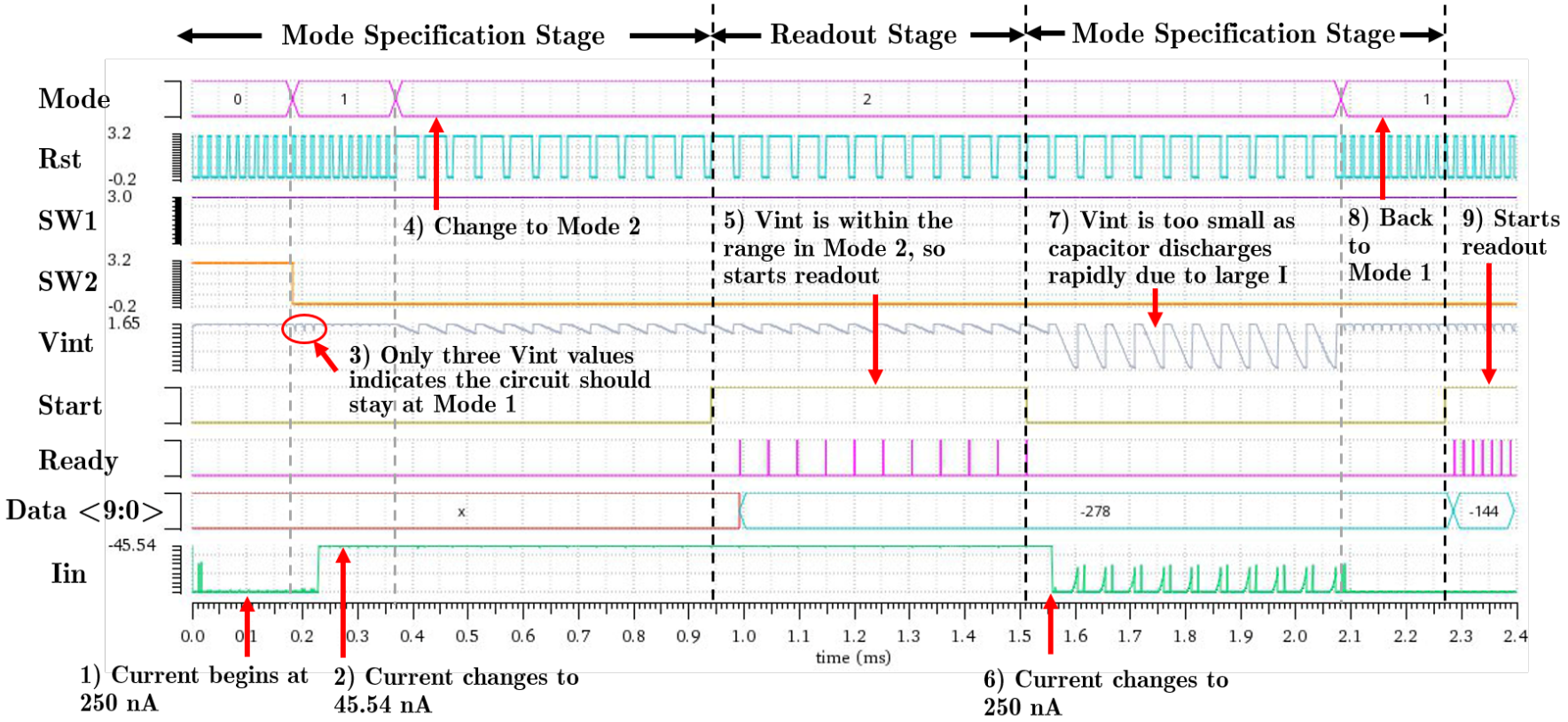


Figure 6.6 Readout circuit operation for a varying input current. The readout circuit transitions to a suitable mode based on the input current and performs ADC conversion during readout stage.

To express the relationship of the mode transition time with respects to the changes in current. A timing diagram in Fig. 6.7 is drawn.

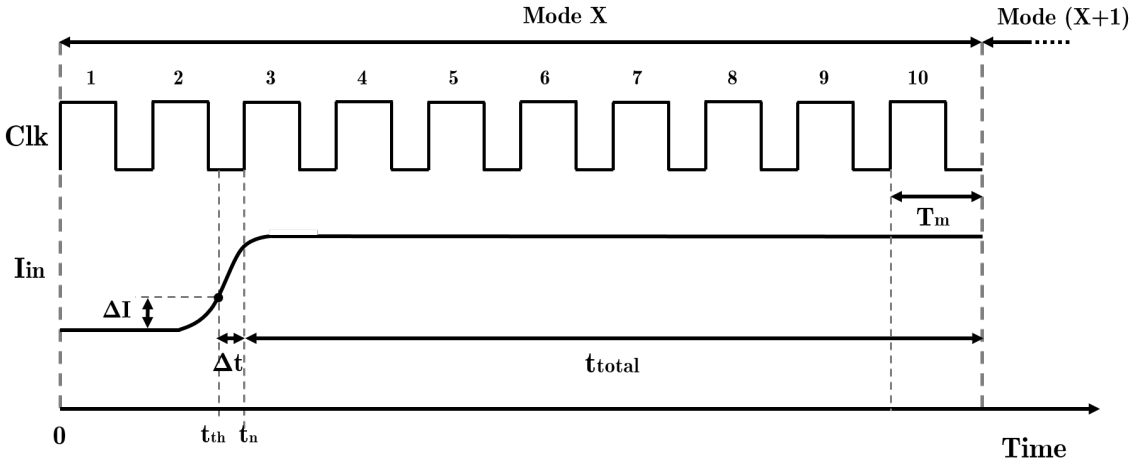


Figure 6.7 Mode transition timing diagram.

The mode transition time is the time taken where for the system to transition to the next mode given the current has reached the current limit of a particular mode. In Fig. 6.7, ΔI is the change in current to the mode limit and Δt is the time taken to the next rising clock edge from the time where current has reached the limit of a mode. Thus, the **single mode transition time**, t_m is given by:

$$t_m = \Delta t + t_{total} \tag{6.13}$$

Since Δt is negligible, thus

$$t_m = t_{total} = (10 - n)T_m \tag{6.14}$$

where n is the n-th rising clock edge and T_m is the period of mode clock cycle. T_m for each mode is given in Table 6.1.

Mode (i)	**0**	**1**	**2**	**3**	**4**	**5**	**6**	**7**
$\boldsymbol{T}_{m(i)}$ **(**$\boldsymbol{\mu}$**s)**	17	17	52	332	2572	20492	20492	163852

Table 6.1 Period of clock cycle for each mode

A general equation for mode transition timing from Mode i to Mode j is given by equation 6.15.

$$t_{m(i-j)} = (10 - n)T_{m(i)} + 10T_{m(i+1)} + ... + 10T_{m(j)} \tag{6.15}$$

A ramp input current is also applied to the system as shown in Fig. 6.8. When the input current is ranging from 1 μA to 8 μA, the system operates in Mode 0. For current lower than 1 μA, the system begins to transition to lower mode. As the input current rises again, the system transitions backward to Mode 0.

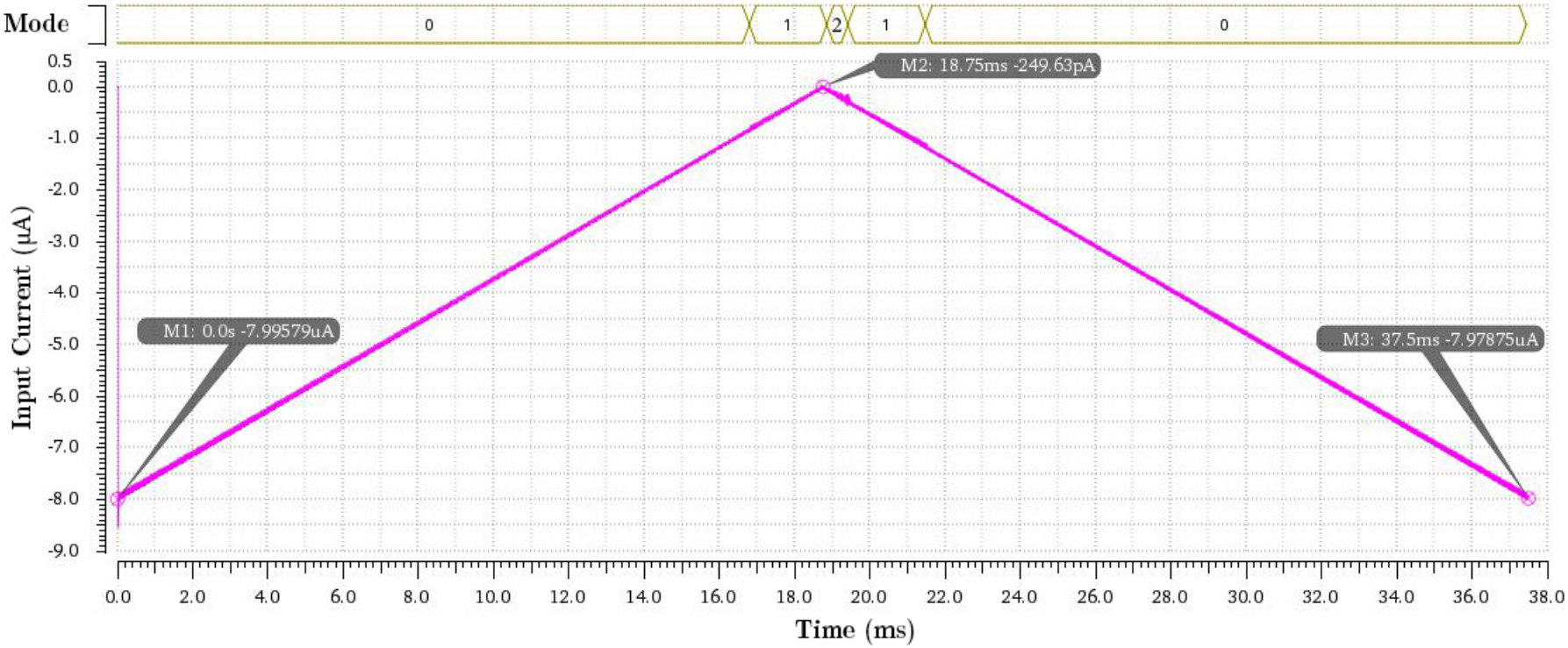


Figure 6.8 Mode transition for ramp input current

6.2 Parametric Simulation

Parametric simulation is performed by varying the input current and plot its operating mode. However, due to extremely long simulation time, the parametric simulation is only carried out up to input current range of Mode 4. The result of the simulation in Fig. 6.9 gives a staircase plot where the operating mode is higher for lower current as expected.

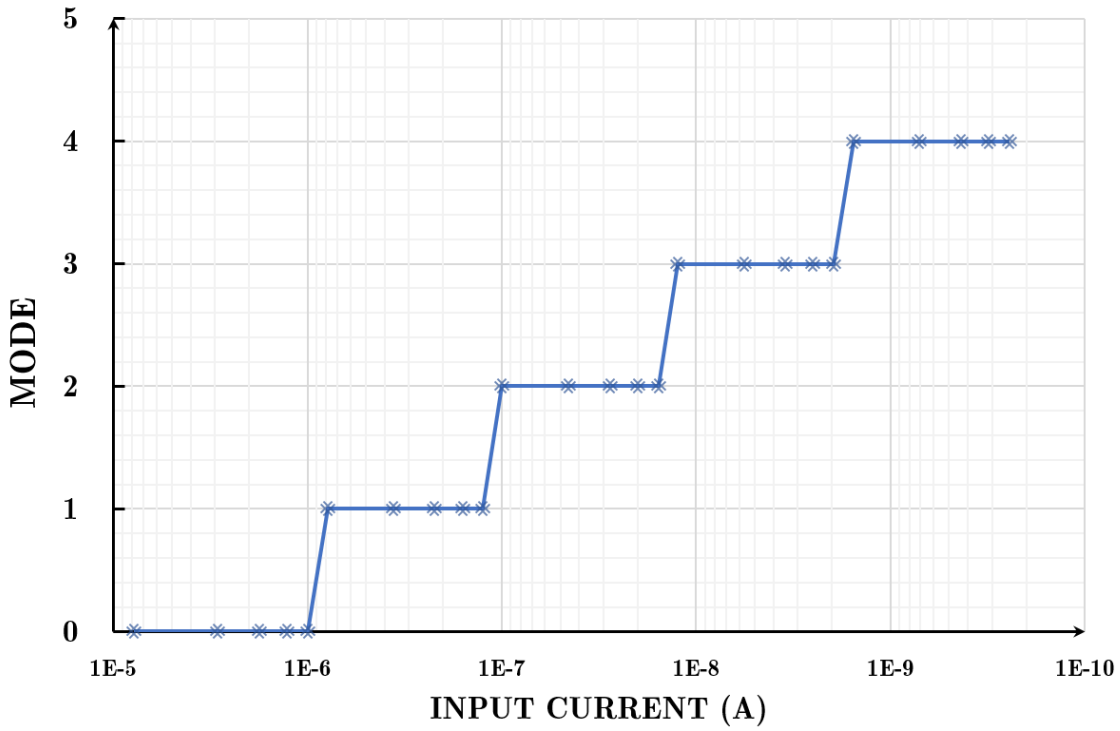


Figure 6.9 Mode versus input current

6.3 Chapter Summary

In this chapter, an overview of the system block diagram is presented. The operation of the readout circuit is demonstrated via transient simulations under different conditions, for example constant, noisy and varying input current. The mode specification stage and readout stage are performed by the readout circuit and a correct ADC output is generated. The mode transition timing equation is also derived and explained to determine the time taken to transition from one mode to the next mode with respect to the changes in input current. Lastly, parametric simulation is performed to show the relationship of mode with input current in which the circuit operates at lower mode for higher current and higher mode for lower current. In a nutshell, the performance of the readout circuit is able to perform autonomous gain control to measure a wide dynamic range of input current and has fulfilled the project goal.

Chapter 7

Layout

In this chapter, the layouts of the analogue and digital part are presented, and the techniques used are described in detail.

7.1 Analogue Layout

The input differential pair of the folded cascode amplifier are split into smaller transistors and then interdigitated in a common-centroid configuration [29], where the PMOS transistors are laid symmetrically about a common center in the layout. This can be seen in the layout of both the switched-capacitor integrator and the sample and hold circuit as illustrated in Fig. 7.1 and Fig. 7.2 respectively. This technique allows the two transistors to cancel process gradient in both the x and y directions and expose both devices to heat source(s) in an identical manner. Thus, the sensitivity due to process variation and mismatch can be reduced. They are also stacked together at their common drain and source to reduce total width of the device. Dummies are also placed at both sides of the differential amplifier. Furthermore, a localised guard rings are used to surround each transistor pair to reduce the substrate noise [30]. All the analogue circuits passed the DRC and LVS rules.

7.2 Digital Layout

The digital circuit layout is carried out using Cadence Genus and Innovus. However, the digital layout is yet to be completed at this stage due to time constraint and lack of technical supports. In addition, this is the first time for the author to do digital layout using Genus and Innovus since previous digital layout is done in Cadence RC complier and Encounter. Nevertheless, the design flow charts of digital synthesis and Place & Route (P&R) are presented in Fig. 7.4 as a reference for future work.

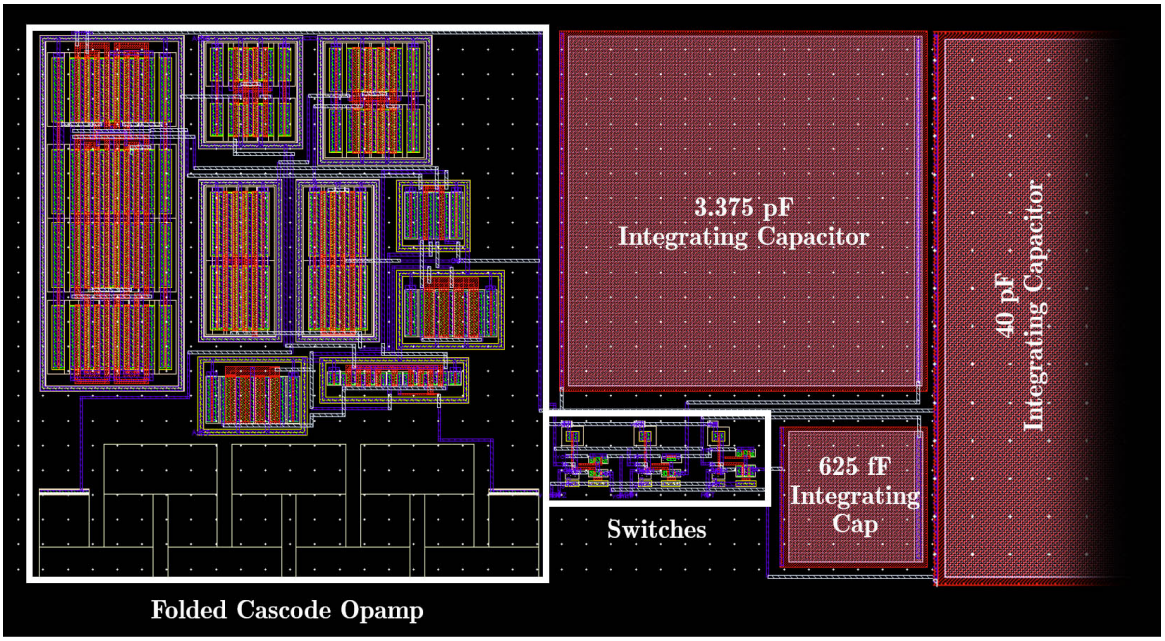


Figure 7.1 Layout for switched capacitor integrator

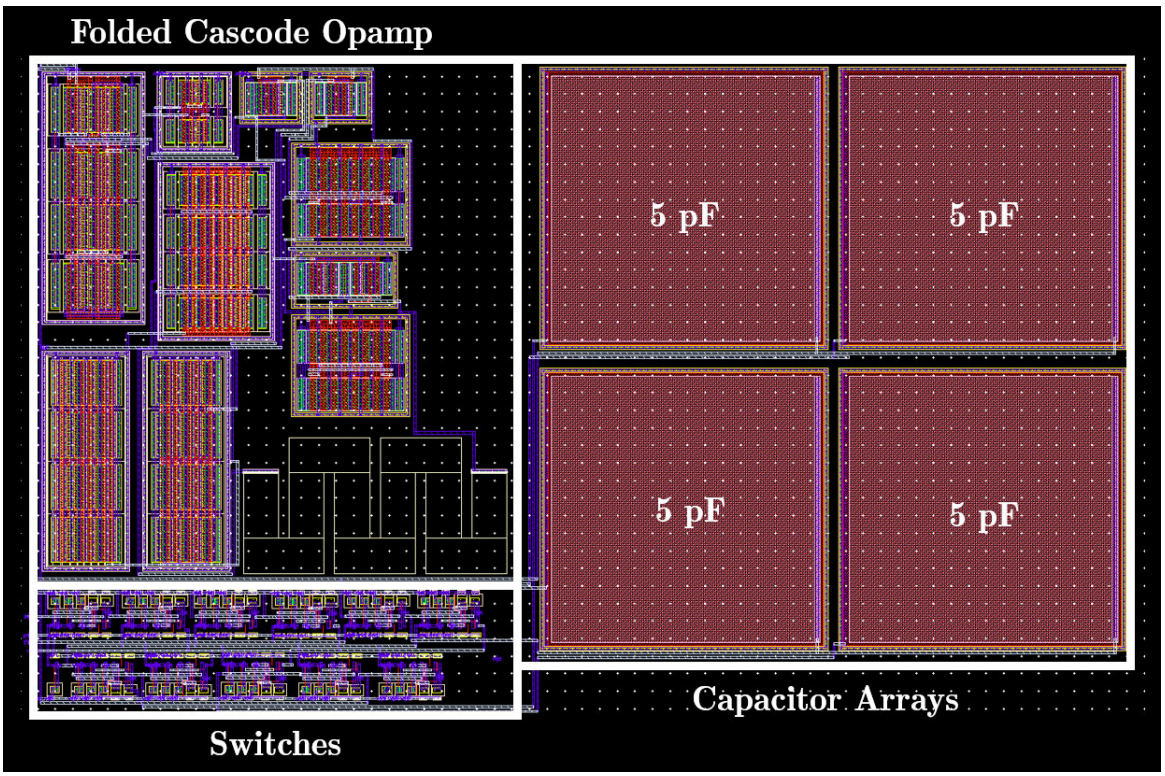


Figure 7.2 Layout of sample and hold circuit

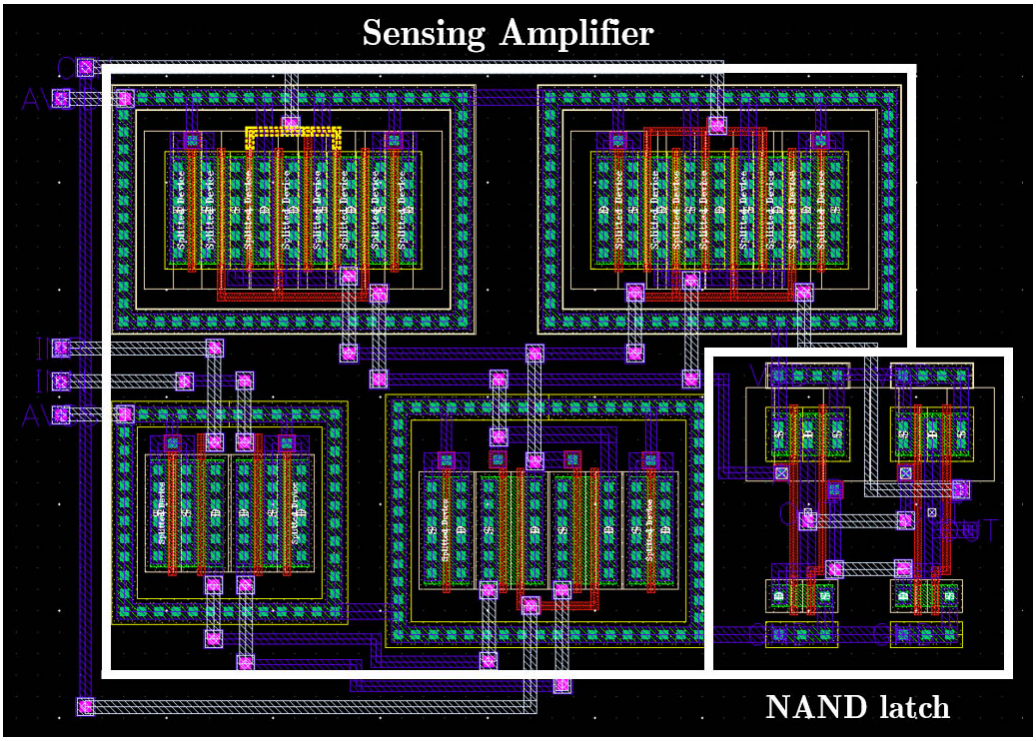


Figure 7.3 Layout of clocked comparator

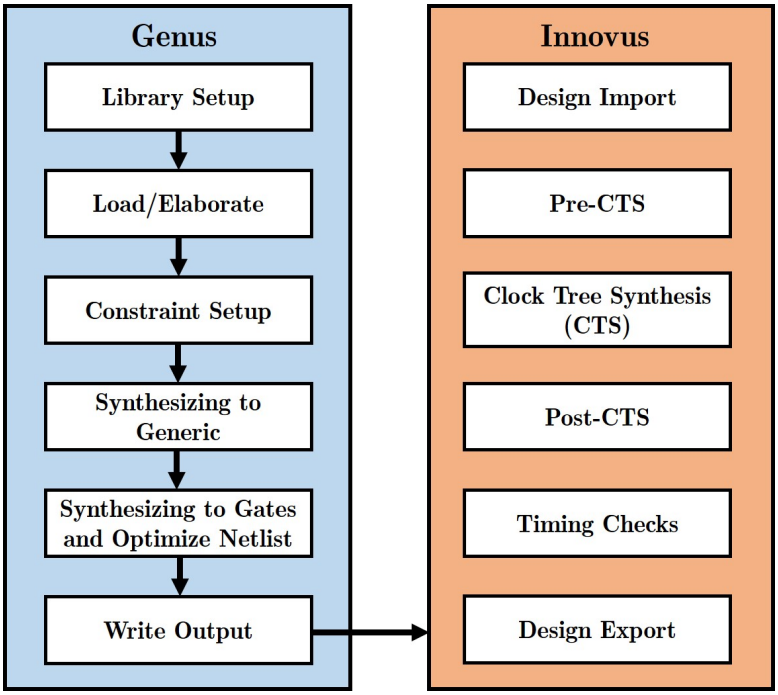


Figure 7.4 Digital synthesis and P&R flow using Genus and Innovus

Chapter 8

Conclusion

8.1 Conclusion

In hindsight, this project was an ambitious undertaking, which required not only a huge number of implementations and modifications of the analogue part, but also the employment of the novel digital circuit which is able to perform autonomous gain control. In addition, there were many challenges faced in this project, for example, improving the accuracy of the analogue part, designing the digital circuit for AGC for the first time, handling Cadence tools for analysis and simulations etc. Ultimately all of them were done successfully, given that individual part of the readout circuit has been shown to operate successfully, and can fulfill all the target specifications. A comparison of the designed readout circuit with the state-of-the-art readout circuits is presented in Table 8.1.

	Circuit Structure	**Current Range**		**Dynamic**	**Autonomous**
		Min	**Max**	**Range**	**Gain**
TCAS'07[5]	Current to Time	1 pA	1 nA	60 dB	No
TBCAS'13[13]	Current to Frequency	24 pA	0.35 μA	83 dB	No
TBCAS'07[7]	Feedback modulated $\Sigma\Delta$	0.1 pA	$\pm$0.5 μA	134 dB	No
TBCAS'16[8]	Input modulated $\Sigma\Delta$	0.1 pA	16 μA	164 dB	No
TBCAS'17[14]	Switched-Capacitor	0.47 pA	$\pm$20 μA	153 dB	No
TCAS'13[9]	Current Conveyor	8.6 pA	$\pm$350 nA	92 dB	No
JCCS'09[15]	Current Preamplifier	1 fA	$\pm$ 1μA	180 dB	No
This work		44 fA	$\pm$ 13 μA	169 dB	Yes

Table 8.1 Comparison between state-of-the-art of the amperometric current readout circuits

The readout circuit introduced in this report can measure currents within $\pm$13 μA with a minimum input-referred noise of 44 fA. The dynamic range of the designed readout circuit is 169 dB. The autonomous gain control system with hysteresis operation was implemented and demonstrated for the first time using simple state machine. The autonomous gain control readout circuit functions well

as a whole, and can potentially expand the market of biosensors significantly. Since biosensor plays a crucial role in personalised health care, the introduction of autonomous gain control can encourage people to use biosensors for their personal healthcare, thus improving their health care quality. It is believed that this project has created the basis of autonomous operation for readout circuits which pushes the boundary of the development of point-of-care diagnostics and the quality of clinical or non-clinical analyses.

8.2 Achievements

At the end of the project, the following tasks were completed:

- Investigate the current preamplifier topology for readout circuits and derive the small-signal relationship of the circuit.
- Implement a readout circuit which is capable of measuring input current with a wide dynamic range.
- Implement a digital circuit to perform autonomous gain control using hardware descriptive language.
- Analyse and simulate the operations of the readout circuit system under different conditions.

8.3 Future Work

While the project mostly focused on the implementations and analysis towards the goals of the project, and has achieved most of the target specifications, there are still a lot of future works that could be done to improve the circuit. Since the project has a deadline, there is a need to definitively decide to stay with the design in order to complete the remaining work in time. Hence, this section will highlight a few possibles further works and suggestions which would be worth investigating.

- Implement an internal system clock generator. Due to time constraint, the internal clock generator is not implemented. This could be done easily by designing an oscillator using a series of inverter. However, more effort should be put to ensure the error in clock is as low as possible since the precision of the switched-capacitor readout circuit is highly dependent on the integration time.
- Implement a system to change the reference voltages for comparator and ADC with respects to the direction of current flows. This can be achieved easily by using another comparator.
- Implement a circuit which gives an accurate reference circuit. Currently, the readout circuit depends on the external reference voltages for the comparator. A voltage regulator could be used to generate the voltage references from VDD or VCM.

- Run simulation using the actual current data points collected from a sensor. Although the readout circuit is tested with different input currents, however it is not sufficient. By running simulation using current generated from sensor can give a more reliable indication of the readout circuit performance.
- Improve the layout of the readout circuit. Although the layout shown in Chapter 7 adapts most of the proper techniques in designing the layout, however, there are still room for improvements For example, split the capacitor into unit capacitance and arrange them in common centroid configuration to reduce mismatch, noise and hence, improve the linearity. Dummy switches and capacitors can be added as well. Extra silicon area can be filled by decoupling capacitor to avoid waste of silicon area and also suppress high frequency noise at the same time. More efforts should be put on the components which will give more parasitic capacitance.

Appendix A

VHDL Code

A.1 Clock Generator

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity freq_select is
port(
  i_clk          : in  std_logic;
  i_rst          : in  std_logic;
  i_select       : in  std_logic_vector(2 downto 0);
  o_clk_div      : out std_logic);
end freq_select;

architecture rtl of freq_select is

signal clk_divider : unsigned(14 downto 0):= "000000000000000";

begin


p_clk_divider: process(i_rst,i_clk)
begin
  if(i_rst='1') then
    clk_divider   <= (others=>'0');
  elsif(rising_edge(i_clk)) then
    clk_divider   <= clk_divider + 1;
  end if;
end process p_clk_divider;

with i_select select
  o_clk_div <= i_clk     when "000",
         clk_divider(2) when "001",
         clk_divider(5) when "010",
```

```
          clk_divider(8)    when "011",
          clk_divider(11)   when "100",
          clk_divider(14)   when "101",
          '0'               when others;
end rtl;
```

A.2 Improved Clock Generator

```
architecture rtl of freq_select is
type state_type is (statehigh, statelow);
signal current_state: state_type;
signal counthigh : integer range 0 to 163841 :=0;
signal countlow : integer range 0 to 11 := 0;
signal cycle_no : integer range 0 to 163841 :=0;

begin

process(i_rst,i_clk, i_select)

begin
  if(i_rst='1') then
    o_clk_out <= '0';

  elsif(rising_edge(i_clk)) then
      if (i_select <= "000") then
        cycle_no <= 5;
      elsif(i_select <= "001") then
        cycle_no <= 5;
      elsif (i_select <= "010") then
        cycle_no <= 40;
      elsif (i_select <= "011") then
        cycle_no <= 320;
      elsif (i_select <= "100") then
        cycle_no <= 2560;
      elsif (i_select <= "101") then
        cycle_no <= 20480;
      elsif (i_select <= "110") then
        cycle_no <= 20480;
      elsif (i_select <= "111") then
        cycle_no <= 163840;
      else
        cycle_no <= 1;
      end if;

    case current_state is
    when statehigh =>
```

```
      if(counthigh < cycle_no - 1) then
        o_clk_out <= '1';
      else
        o_clk_out <= '1';
        current_state <= statelow;
        countlow <= 0;
      end if;
      counthigh <= counthigh + 1;

    when statelow =>
      if(countlow < 11) then
        o_clk_out <= '0';
        countlow <= countlow + 1;
      else
        o_clk_out <= '0';
        current_state <= statehigh;
        counthigh <= 0;
      end if;

    end case;
  end if;
end process;
end rtl
```

A.3 Autonomous Gain Control

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity agc_algorithm is
port (
  clk : in std_logic;
  reset : in std_logic;
  comp_max : in std_logic;
  comp_min : in std_logic;
  start : out std_logic;
  sw1 : out std_logic;
  sw2 : out std_logic;
  frequency: out std_logic_vector(2 downto 0);
  limit_ind : out std_logic);
end entity agc_algorithm;

architecture structural of agc_algorithm is
  type state_type is (s0,s1,s2,s3,s4,s5,s6,s7,readout); --state declaration
  signal current_s, previous_s: state_type;
```

```
  signal count_check: integer range 0 to 10 :=0;
  signal count_highstate: integer range 0 to 10 :=0;
  signal count_lowstate: integer range 0 to 10 :=0;
  signal count_readout: integer range 0 to 10 :=0;
  signal count_data: integer range 0 to 11 :=0;

begin
--clocked part
process (clk, reset, comp_max, comp_min)
  variable threshold : natural range 0 to 10 := 5;

begin
  if (reset='1') then
    current_s <= s4;  --default state on reset

  elsif (rising_edge(clk)) then
    limit_ind <= '0';
    if (previous_s = current_s) then
      threshold := 3;
    else
      threshold := 5;
    end if;

    case current_s is

    ----------------------Mode 0: Period: 10us Capactior: 40pF----------------------
    when s0 =>

      sw1 <= '1';
      sw2 <= '1';
      frequency <= "000";

      if(count_check = 10) then
        if (count_readout > threshold) then
          current_s <= readout;
        elsif (count_highstate > 10-threshold) then
          current_s <= s1;
        elsif (count_lowstate > 10-threshold) then
          limit_ind <= '1';
          current_s <= s0;
        end if;
        count_readout <= 0;
        count_highstate <= 0;
        count_lowstate <= 0;
        count_check <= 0;
        previous_s <= current_s;

      else
        if ((comp_max = '0') AND (comp_min = '0')) then
          count_readout <= count_readout + 1;
```

```
71          elsif (comp_max = '0' AND comp_min = '1') then
72            count_highstate <= count_highstate + 1;
73          elsif (comp_max = '1' AND comp_min = '0') then
74            count_lowstate <= count_lowstate + 1;
75          end if;
76          count_check <= count_check + 1;
77        end if;
78        start <= '0';
79
80      ----------------------Mode 1: Period: 10us Capactior: 5pF----------------------
81      when s1 =>
82        sw1 <= '1';
83        sw2 <= '0';
84        frequency <= "000";
85
86        if(count_check = 10) then
87          if (count_readout > threshold) then
88            current_s <= readout;
89          elsif (count_highstate > 10-threshold) then
90            current_s <= s2;
91          elsif (count_lowstate > 10-threshold) then
92            current_s <= s0;
93          end if;
94          count_readout <= 0;
95          count_highstate <= 0;
96          count_lowstate <= 0;
97          count_check <= 0;
98          previous_s <= current_s;
99
100       else
101         count_check <= count_check + 1;
102         if (comp_max = '0' AND comp_min = '0') then
103           count_readout <= count_readout + 1;
104         elsif (comp_max = '0' AND comp_min = '1') then
105           count_highstate <= count_highstate + 1;
106         elsif (comp_max = '1' AND comp_min = '0') then
107           count_lowstate <= count_lowstate + 1;
108         end if;
109       end if;
110       start <= '0';
111
112     ----------------------Mode 2: Period: 80us Capactior: 5pF----------------------
113     when s2 =>
114       sw1 <= '1';
115       sw2 <= '0';
116       frequency <= "001";
117
118       if(count_check = 10) then
119         if (count_readout > 5) then
120           current_s <= readout;
```

```
121         elsif (count_highstate > 5) then
122           current_s <= s3;
123         elsif (count_lowstate > 5) then
124           current_s <= s1;
125         end if;
126         count_readout <= 0;
127         count_highstate <= 0;
128         count_lowstate <= 0;
129         count_check <= 0;
130         previous_s <= current_s;
131 
132       else
133         if (comp_max = '0' AND comp_min = '0') then
134           count_readout <= count_readout + 1;
135         elsif (comp_max = '0' AND comp_min = '1') then
136           count_highstate <= count_highstate + 1;
137         elsif (comp_max = '1' AND comp_min = '0') then
138           count_lowstate <= count_lowstate + 1;
139         end if;
140         count_check <= count_check + 1;
141       end if;
142       start <= '0';
143 
144     ----------------------Mode 3: Period: 640us Capactior: 5pF----------------------
145     when s3 =>
146       sw1 <= '1';
147       sw2 <= '0';
148       frequency <= "010";
149 
150       if(count_check = 10) then
151         if (count_readout > 5) then
152           current_s <= readout;
153         elsif (count_highstate > 5) then
154           current_s <= s4;
155         elsif (count_lowstate > 5) then
156           current_s <= s2;
157         end if;
158         count_readout <= 0;
159         count_highstate <= 0;
160         count_lowstate <= 0;
161         count_check <= 0;
162         previous_s <= current_s;
163 
164       else
165         if (comp_max = '0' AND comp_min = '0') then
166           count_readout <= count_readout + 1;
167         elsif (comp_max = '0' AND comp_min = '1') then
168           count_highstate <= count_highstate + 1;
169         elsif (comp_max = '1' AND comp_min = '0') then
170           count_lowstate <= count_lowstate + 1;
```

```
171           end if;
172           count_check <= count_check + 1;
173         end if;
174         start <= '0';
175
176       ----------------------Mode 4: Period: 5.12ms Capactior: 5pF----------------------
177       when s4 =>
178         sw1 <= '1';
179         sw2 <= '0';
180         frequency <= "011";
181
182         if(count_check = 10) then
183           if (count_readout > 5) then
184             current_s <= readout;
185           elsif (count_highstate > 5) then
186             current_s <= s5;
187           elsif (count_lowstate > 5) then
188             current_s <= s3;
189           end if;
190           count_readout <= 0;
191           count_highstate <= 0;
192           count_lowstate <= 0;
193           count_check <= 0;
194           previous_s <= current_s;
195         else
196           if (comp_max = '0' AND comp_min = '0') then
197             count_readout <= count_readout + 1;
198           elsif (comp_max = '0' AND comp_min = '1') then
199             count_highstate <= count_highstate + 1;
200           elsif (comp_max = '1' AND comp_min = '0') then
201             count_lowstate <= count_lowstate + 1;
202           end if;
203           count_check <= count_check + 1;
204         end if;
205         start <= '0';
206
207       ----------------------Mode 5: Period: 40.96ms Capactior: 5pF----------------------
208       when s5 =>
209         sw1 <= '1';
210         sw2 <= '0';
211         frequency <= "100";
212
213         if(count_check = 10) then
214           if (count_readout > 5) then
215             current_s <= readout;
216           elsif (count_highstate > 5) then
217             current_s <= s6;
218           elsif (count_lowstate > 5) then
219             current_s <= s4;
220           end if;
```

```
221         count_readout <= 0;
222         count_highstate <= 0;
223         count_lowstate <= 0;
224         count_check <= 0;
225         previous_s <= current_s;
226       else
227         if (comp_max = '0' AND comp_min = '0') then
228           count_readout <= count_readout + 1;
229         elsif (comp_max = '0' AND comp_min = '1') then
230           count_highstate <= count_highstate + 1;
231         elsif (comp_max = '1' AND comp_min = '0') then
232           count_lowstate <= count_lowstate + 1;
233         end if;
234         count_check <= count_check + 1;
235       end if;
236       start <= '0';
237
238     ----------------------Mode 6: Period: 40.96ms Capactior: 625fF----------------------
239     when s6 =>
240       sw1 <= '0';
241       sw2 <= '0';
242       frequency <= "100";
243
244       if(count_check = 10) then
245         if (count_readout > 5) then
246           current_s <= readout;
247         elsif (count_highstate > 5) then
248           current_s <= s7;
249         elsif (count_lowstate > 5) then
250           current_s <= s5;
251         end if;
252         count_readout <= 0;
253         count_highstate <= 0;
254         count_lowstate <= 0;
255         count_check <= 0;
256         previous_s <= current_s;
257       else
258         if (comp_max = '0' AND comp_min = '0') then
259           count_readout <= count_readout + 1;
260         elsif (comp_max = '0' AND comp_min = '1') then
261           count_highstate <= count_highstate + 1;
262         elsif (comp_max = '1' AND comp_min = '0') then
263           count_lowstate <= count_lowstate + 1;
264         end if;
265         count_check <= count_check + 1;
266       end if;
267       start <= '0';
268
269     ----------------------Mode 7: Period: 327.68ms Capactior: 625fF----------------------
270     when s7 =>
```

```
271         sw1 <= '0';
272         sw2 <= '0';
273         frequency <= "100";
274 
275         if(count_check = 10) then
276           if (count_readout > 5) then
277             current_s <= readout;
278           elsif (count_highstate > 5) then
279             current_s <= s7;
280           elsif (count_lowstate > 5) then
281             current_s <= s6;
282           end if;
283           count_readout <= 0;
284           count_highstate <= 0;
285           count_lowstate <= 0;
286           count_check <= 0;
287           previous_s <= current_s;
288         else
289           if (comp_max = '0' AND comp_min = '0') then
290             count_readout <= count_readout + 1;
291           elsif (comp_max = '0' AND comp_min = '1') then
292             count_highstate <= count_highstate + 1;
293           elsif (comp_max = '1' AND comp_min = '0') then
294             count_lowstate <= count_lowstate + 1;
295           end if;
296           count_check <= count_check + 1;
297         end if;
298         start <= '0';
299 
300       ----------------------Readout Stage----------------------
301       when readout =>
302         if (count_data < 10) then
303           start <= '1';
304           count_data <= count_data + 1;
305           current_s <= readout;
306         else
307           current_s <= previous_s;
308           count_data <= 0;
309         end if;
310       end case;
311 
312     end if;
313 end process;
314 end;
```

Listing A.1 VHDL code for Gain Control Algorithm

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