AN AUTOMATIC-GAIN-CONTROL (AGC) CIRCUIT FOR ELECTROCHEMICAL SENSORS

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B.Eng in Electrical Engineering

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Abstract

Today many medical devices are based on biosensors. Biosensors use electrochemical detection to measure the concentration of specific metabolites which characterize patients with chronical conditions. One of the most important and interesting metabolites is glucose as it is a marker for diabetes.

The most significant component of a biosensor is the potensiostat. The potensiostat is the fundamental part of electrochemical sensing and it is a device that measures the concentration of the metabolite in a chemical solution. It uses three electrodes which interact with the chemical solution. These three electrodes of the potensiostat contact the analyte which contains the specific metabolite.

This thesis describes the design of novel automatic glucose sensing integrated circuit for Diabetes management. The implemented circuitry uses chronoamperomentry measurements. The design consists of a readout part which measures the concentration of the metabolite and a feedback part which adjust properly the readout part. By doing that, has been achieved an automatic adjustment of the measuring requirements. Therefore, the measuring takes place automatically for a wide range of glucose concentrations. The design has been implemented using a .35 m standard CMOS technology.

There is a variety of techniques used to implements Readout topologies. Furthermore, there are already designed Readout topologies based on the same principle as the one presented here. However, this is a first time that a readout circuit can autonomously modify its properties in order to be able to detect the amount of the metabolite in accuracy.

Acknowledgment

I would like to express my gratitude to all the people that guided or advised me during my project. First and foremost, I would like to thank my supervisor Dr Sara S. Ghoreishizadeh for the help, guidance and inspiration. I am indebted to her for all the time she spent explaining me the concepts of bio sensing. I learned from her and through the project she proposed how to analyze and interpret Analogue circuits and how to understand the practical functionality of them.

I wish to thank also Dr Pantelis Georgiou. The group meetings he organized gave me vital feedback and guided me to take the right decisions. Meeting with the people from the bio-inspired group and the other MSc students was both inspiring and extremely useful. There I had the opportunity to be exposed to many real-time discussions related to problems and issues of my thesis.

Also, I would really like to thank all my friends and my roommates that supported me during this year. Spending time with people I appreciate and respect were the breaks I needed to charge my batteries. Being with them or speaking through Skype could take my mind off my workload for a little bit and that helped me maintain a balance and forget about my issues.

Finally, I would like to express my gratefulness to my family. My parents and my brother where supporting me through my whole MSc. They were always there for me through the encouragement and condence they gave me.

Contents

List of Figures

List of Tables

Abbreviations

ADC: Analog to digital converter

DAC: Digital to analog converter

CA: Chronoamperometry

CE: Counterelectrode

CV Counterelectrode

WE Workingelectrode

TIA Tansimpedance amplifier

CGTIA Common-Gate tansimpedance amplifier

CYP CytochromeP450

Chapter 1

Introduction

NO wadays a part of clinical analysis can be replaced by the personalized medicine. That is beneficial for the patients as the personalized medicine enhance the quality of the treatment because it provides faster test results and reduces the cost of the clinical analysis. One of the most important aspects of personalized medicine is the effective monitoring of human metabolism [8]. The reason for that is that many chronical diseases are related to endogenous metabolites like glucose, lactate or ATP. So electrochemical detection of metabolites is a matter of great importance.

1.1 Motivation

Electrochemical detection is conducted by electrochemical sensors. These are devices that can perform measurements of specific metabolites in blood very fast and accurate [9]. Being able to track real-time changes in the concentration of specific metabolites in blood provides information related to the health condition of the patient. Furthermore, by real-time monitoring sudden incidents can be prevented.

The main devices that conduct electrochemical detection are the biosensors. Many biosensors use Chronoamperometry. This is a widely used electrochemical technique to measure the concentration of endogenous molecules like glucose. The biosensor is using three electrodes [2] that contact the analyte which contains a specific metabolite. Those

are the working electrode that applies a specific voltage to the analyte, the reference electrode which act as reference without passing any current and the counter electrode that passes the current that flows to the working electrode. The magnitude of that current is proportional to the concentration of the metabolite inside the analyte.

There are many different designs of readout circuits that manage to track the concentration of endogenous molecules like glucose using Chronoamperometry. Using different techniques, they manage to effectively measure the current that flows to the working electrode and indicates the concentration of the metabolite. However, they all suffer from a common limitation. That is that even the state of the art readout circuits can measure only a small range of currents without manual modification of the measuring scale. That lack of autonomy makes the readout circuits more complex for the user and set and important limit to the creation of handy biosensors.

1.2 Challenges

The main challenges related to this thesis are listed below.

- The derivation of an effective readout circuit and a sample and hold circuit to measure the current generated by the biosensor.
- The switch timing organization to limit charge injection issues and ensure correct measurement.
- The implementation of the derived circuit in a way to avoid instability issues.
- The design of digital circuit as a feedback of the readout circuit using a hardware description language and then implementation of that circuit using standard cells.
- The management of interaction between the readout part and the feedback digital part.
- The linearity of the measurements corresponding to the respective readout currents.
- The optimization of the whole circuitry in terms of power consumption and area.

1.3 Thesis Outline

Chapter 2 goes through the electrochemical sensing strategies for detection of human metabolites. Also it includes an overview of the control and readout circuits related to amperometric electrochemical sensors that have been used in the past.

Chapter 3 decribes the inital architecture that has been derived. The main parts of the design are explained. After that are pointed out the limitations of the specific design in terms of stability and measurment range. Moreover, are proposed solutions for each one of the limitations. From these proposed sloutions a new tologoly derives which is explained in detain in the next chaplter.

Chapter 4 presents the parts of the circuit propsed at Chapter 3 in detail. More specific, a descripition of the components that consist the Analogue readout circuit takes place. After that is introduced a new techinique that cancels out a voltage offset drop that happens at a very important node of the Analogue circuit for a specific range of input currents. Finally is presented the timing managment of the switches of the circuit and is given an operating example of the whole Analogue system.

Chapter 5 describes the Digital block of the topology. Intially is explained why a digital block is need. After that are specified the required characteristics of the Digital block. In the end are explained some modification tha took place at the Digital block in order to improve the efficiency of the feedback that it offers.

Chapter 6 Includes the description of the whole system. A whole system simulation example is presented and explained in detail. Conduction of Monte carlo testing is presented and modifications in order to improve the performance in terms of variations are explained. Finally is presented the Layout of the whole chip desiged and a postlayout simulation takes place.

Chapter 7 Summarises what has been concluded from this thesis. It points out the achievements that have been accomplished and the future work that could be done based on them.

Chapter 2

Electrochemical Sensing - State of the Art

2.1 Electrochemical detection

EL ectrochemical detection is commonly used nowadays to effectively monitor patients who suffer from chronic conditions. The electrochemical detection is conducted by biosensors. Widely used is the glucose biosensor for diabetes treatment. Glucose biosensor breaks down the blood glucose which releases electrons which are measured by a potensiostat [10].

Monitoring glucose is important as it is a marker for diabetes. Except glucose there are many other endogenous metabolites which contain information related to other conditions. Characteristic examples are glutamate and cholesterol. Glutamate [11] is the anion of glutamic acid and it is a neurotransmitter. Cholesterol [12] is very important to be monitored as it can cause serious brain damage if it accumulates outside the cells which can happen at brain injuries. Furthermore cholesterol is a lipid molecule which concentration in blood is it closely related to atherosclerosis. Moreover, there are several exogenous metabolites that can provide useful information in drug therapy. Ftorafur, cyclosposamide, ifosfamide and many more are used in chemotherapy treatments. So, monitoring their level in blood during the treatment process can give an indication on

how the body metabolizes the drugs.

2.2 Electrochemical sensing principles

Specific kind of enzymes participate as probes at the monitoring of metabolites at endogenous or exogenous molecules. The oxidases proteins are used in endogenous metabolites detection. More specific, the Oxidases [1] are integrated in the enzyme to cause a redox reaction. The cytochromes P450 are used for exogenous metabolites detection [1] and also participate to a redox reaction.

There are two well know techniques to measure the redox currents that correspond to the metabolite concentration. Cyclic voltammetry and Chronoamperometry. At Cyclic voltammetry [13] there is a potential sweep from an initial value up to a specific value and then back to the initial value again. The current generated is monitored during that process. At the Chronoamperometry there is a constant potential applied and the current generated is monitored.

2.3 Design of the sensor

Chronoamperometry and Cyclic voltammetry are conducted through the electrode based electrochemical cell which uses three electrodes and a potentiostat to apply the voltages required. These three electrodes [14] are the working electrode (WE), the counter electrode (CE) and the reference electrode (RE). The working electrode contacts the analyte and applies a specific voltage to it. Furthermore, through the working electrode flows the measuring current from and to the analyte. The reference electrode applies a reference voltage to the analyte without conducting any current. The counter electrode provides the analyte with current to balance the current dragged by the working electrode.

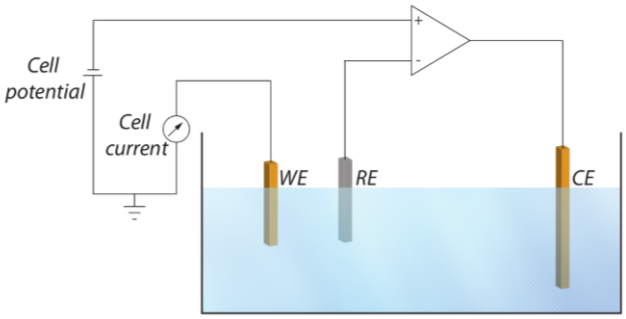

Figure 2.1: three-electrode based electrochemical cell with a potentiostat. Reprinted from [1]

2.4 Integrated circuits for amperometric biosensors

Fig. 2.2 depicts the general simplified topology of a standard readout electronic circuit used for amperometric sensing. The readout circuit amplifies properly the readout current using a trans-impedance amplifier (TIA) and then it digitizes the result with an analog to digital converter (ADC).

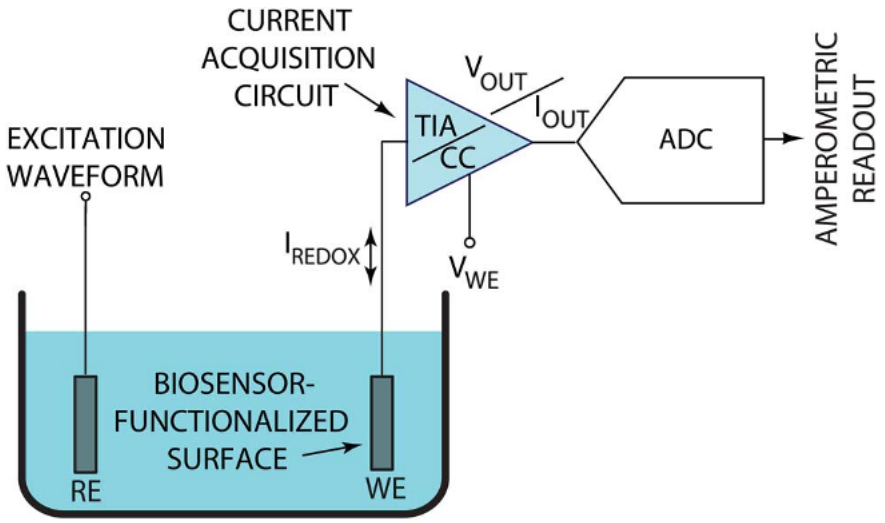

Figure 2.2: Electrochemical amperometric sensory system. Reprinted from [2]

2.5 Current-mode circuits

Many amperometric sensing topologies are based on current mode circuits [15], [16], [17]. The common figure at most of these topologies is the existence of a differential amplifier, usually a common-gate-transimpedance amplifier (CGTIA). The functionality of it is to maintain the voltage at the WE and at the same time to read the current flowing at the WE.

Fig. 2.3 presents the basic readout toplogy based on the CGTIA. As it can be seen the concept is that a reference voltage is aplied to the WE. That creates a current which flows through the transistor M1 and its magnitude expresses the concentration of the metabolite. Using other topologies the read-out current is converted into voltage or into frequency of into time.

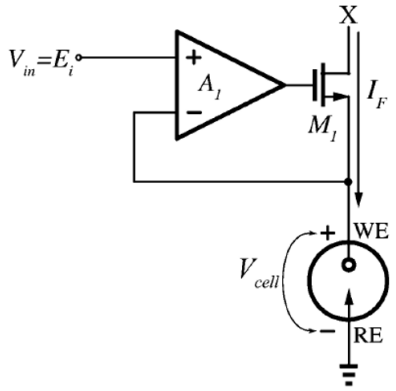

Figure 2.3: readout toplogy based on the CGTIA. Reprinted from. [3]

The read-out current flowing at the Working electrode Fig. 2.3 can be converted into frequency using a topology like Fig. 2.4. As it can be seen, an indectical to the read-out current is given as an input to a relaxation oscillator [4] Fig. 2.5. It produces pulses with frequency proportional to the magnitude of the readout current. Generally the current to frequency circuits consume relitvely low power as there is no need for an ADC. Their main disadvantage is the difficulty of measuring the generated output frequency.

At Fig. 2.6 [5] the read-out current flowing at the Working electrode can be converted into voltage. As it can be seen, the read-out current is being mirrored using a

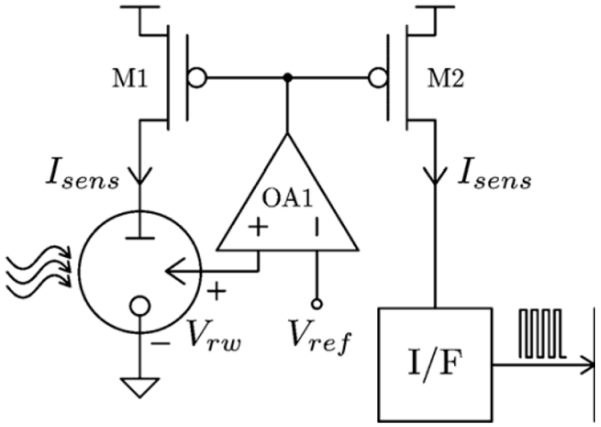

Figure 2.4: Readout current to frequency converter. [3]

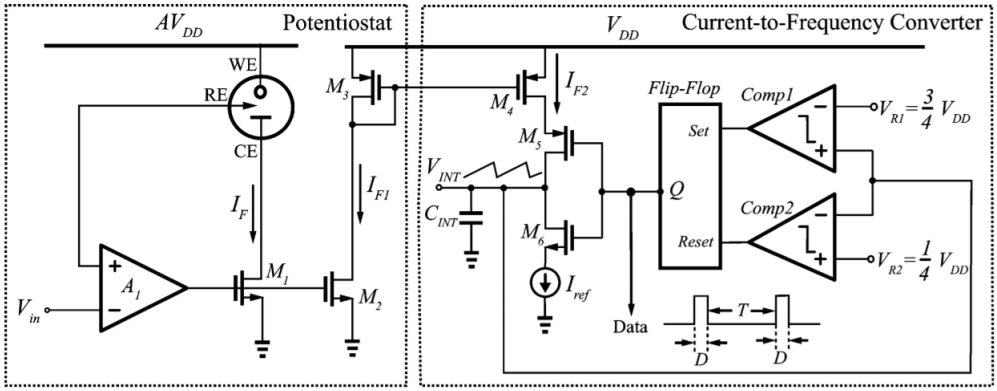

Figure 2.5: Pulse generation with relaxation oscillator. [4]

Wilson mirror topology. That creates a voltage related to the mirrored current which is being amplified with an Opamp. The output of the opamp is a voltage proportional to the read-out current.

Sigma Delta modulator based circuits

The Sigma Delta modulator based readout circuits is a special category of current mode readout circuits. Those circuits manage to achieve a good input dynamic range. Their main characteristic is the ability to provide digital interpretation of the read-out current using current [6] and voltage mode ADC. Fig. 2.7 presents a chracteristic exmple of Sigma Delta modulator based readout circuits where at the feedback loop there is a single-bit deltasigma modulator. That modulator implements an incremental analog-to-

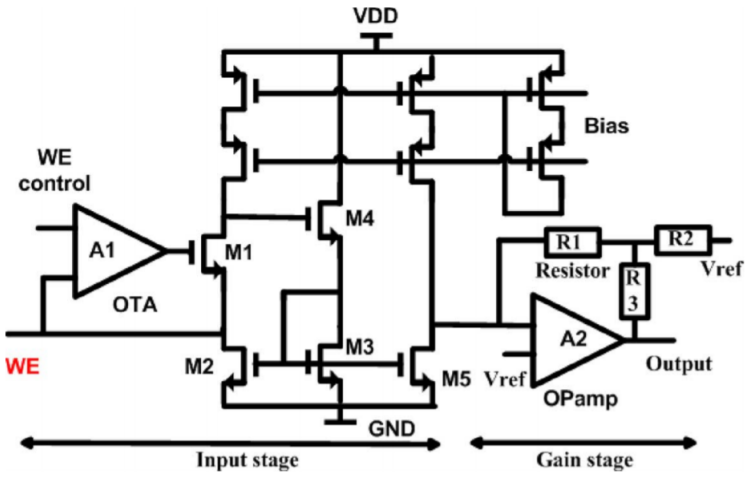

Figure 2.6: Readout current to voltage converter. Reprinted from. [5]

digital converter which generates a digital output that reprsents the read-out current.

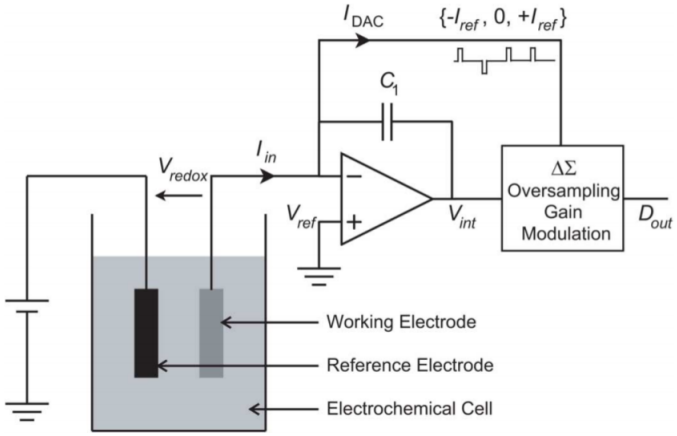

Figure 2.7: Sigma Delta modulator based readout circuits. Reprinted from. [6]

2.6 Voltage-mode circuits

The other main category of circuits used for redox current characterization is the voltage-mode circuits [18], [19]. Fig. 2.8 presents a voltage mode readout circuit [7] which uses a resistive Transimpedance amplifier. At Fig. 2.8 there is a potentiostat which sets a specific potential to the WE and RE. The redox current flows at the feedback resistance of the Transimpedance amplifier which output is a voltage proportional to the redox current.

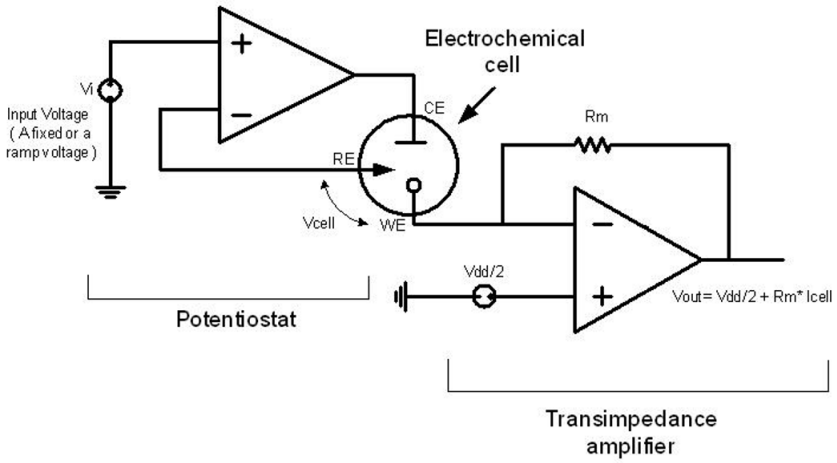

Figure 2.8: Readout current to voltage converter. Reprinted from. [7]

Another approach used at the voltage-mode circuits is to integrate the redox current using a switched-capacitor integrator instead of a resistor at the feedback loop of the Transimpedance amplifier [20], [21].Fig. 2.9 is an indicative example of that. As it can be seen there are three different stages at the topology. Initially there is a SC-integrator which integrates the redox current and converts it into voltage. That voltage is an input to a programmable gain amplifier which output is provided to a sample and hold topology. The held voltage can be input to an analogue to digital converter (ADC).

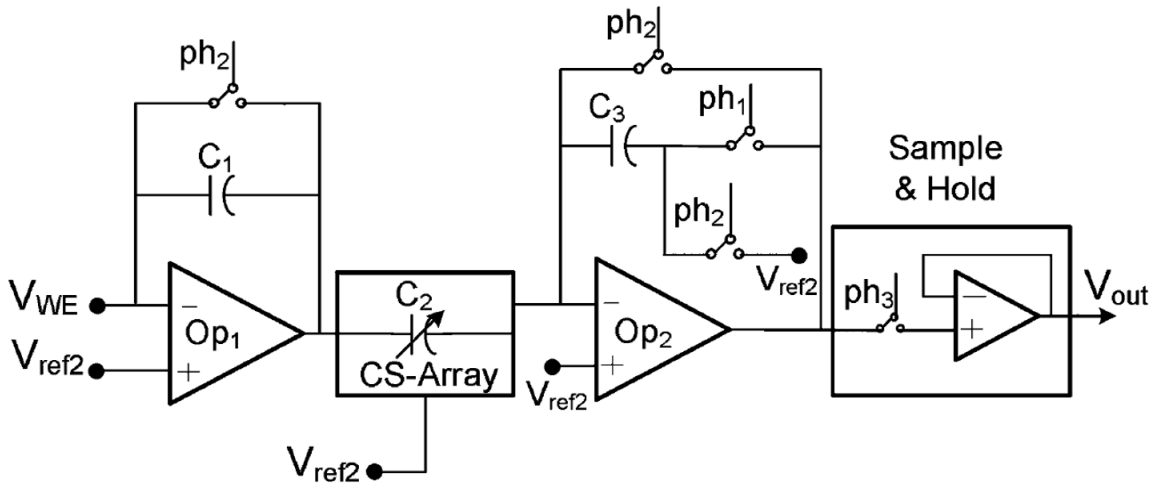

Figure 2.9: Switched-capacitor readout circuit . Reprinted from. [7]

2.7 Comparison

At Table 4.1 are presented the main characteristics of the state-of-the-art integrated readout circuits for amperometry biosensors and also the characteristics of the topology derived from that thesis. As it can be seen the integrated circuit designed is the first and only that can measure the whole range automatically.

Topology	mode	Min	Max	Tech.	Power	Automatic measurment
TBCAS13[20]	single	24 pA	0.35 A	0.35 m	0.19 mW	NO
TBCAS16[21]	single	0.5 A	0.7 A	0.18 m	0.07 mW	NO
TCAS-I06[22]	single	0.05 pA	0.1 A	0.5 m	11 W	NO
TBCAS07[23]	single	0.1 pA	0.5 A	0.5 m	1.27 mW	NO
TBCAS16[12]	single	0.1 pA	16 A	0.5 m	241 W	NO
This work	diff.	86 pA	100 A	0.35 m	4.85 mW	YES

Table 2.1: State-of-the-art readout implementations used in biosensing.

Chapter 3

Core Architecture

3.1 Targets of the design

MAIN purpose of the architecture derived is the ability to measure the current that flows through the working electrode. That can happen by integrating that current onto a capacitance for a specific period of time and measuring the voltage of that capacitance. That voltage is proportional to the current integrated. So a general picture of the topology needed is the one at Fig. 3.1.

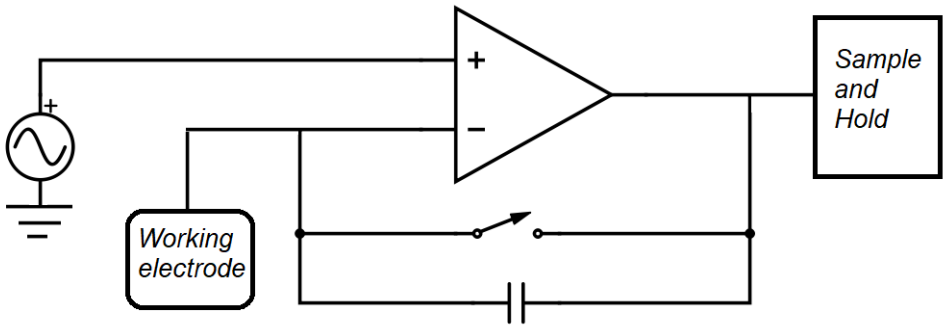

Figure 3.1: Integration topology.

There are two stages. The integration stage and the sample and hold stage. The integration takes place using a differential amplifier. It is used to maintain a steady voltage at the negative node and let the current flow from that node to the working electrode or

from the working electeode to the capacitance. As a result, the same current flows at the right plate of the capacitance at Fig. 3.1 and therefore the current is integrated. After that there is a sample and hold circuitry that holds the measured voltage steady for a specific period of time.

3.2 Initial architecture

Initially the architecture that has been proposed is the following.

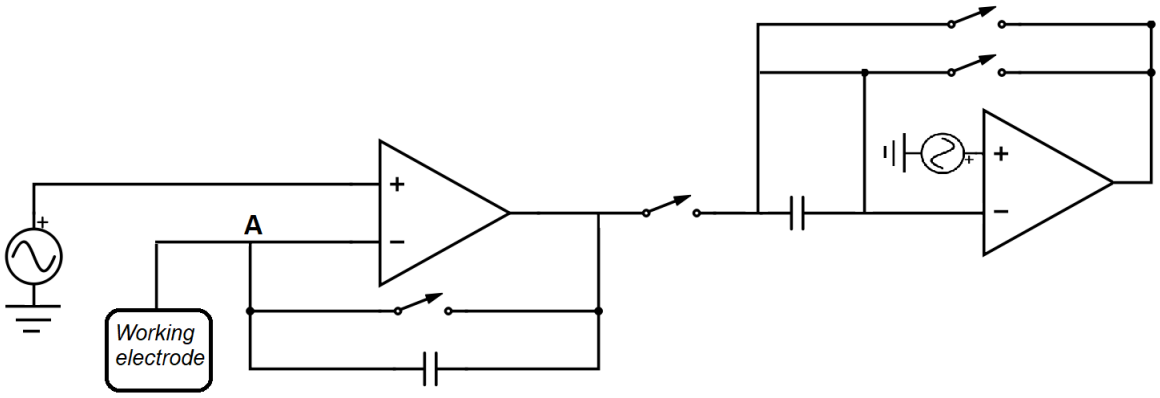

Figure 3.2: First proposed architecture.

The integration of the current takes place through a two-stage differential amplifier Fig. 3.3. The negative input of the differential amplifier is connected to the Working electrode and the positive input to the reference voltage 1.65 V. The working electrode has been simulated using a resistor in parallel with a very big capacitor (10nF).

According to topology at Fig. 3.2, the voltage at node A is kept steady at 1.65V as the amplifier buffers the voltage from the positive to the negative node. At the same time, a current flows from the node A (1.65V) to the working electrode. Therefore, the same amount of current is integrated at the right plate of the capacitance. As a result, the integration that takes place at the right plate of the capacitance is linear (given that the 10nF capacitance is charged) and proportional to the resistance of the working electrode which is proprtional to the concentration of the metabolite Fig. 3.4.

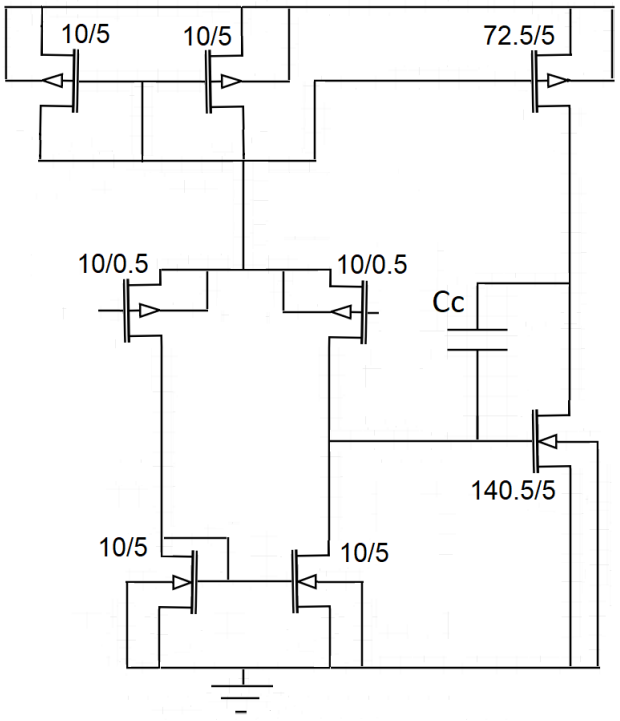

Figure 3.3: Two stage differential amplfier.

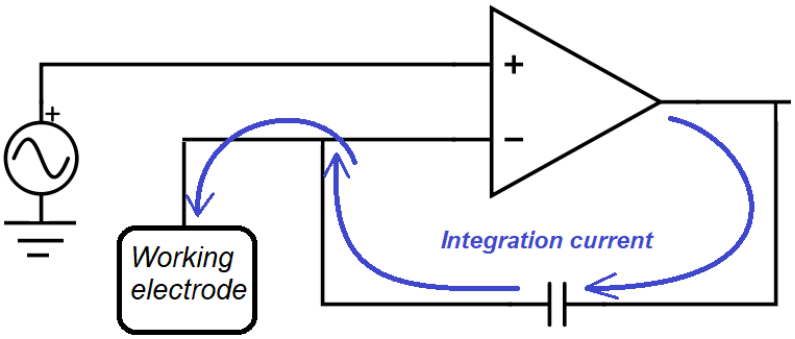

Figure 3.4: Addition of integrating capacitance.

Also, by adding a switch in parallel with the capacitance Fig. 3.5 the integration time can be defined. When the switch is off the current flows through the capacitance and therefore the integration takes place. When the switch is on the current flows through the switch and the integration stops, leading to a steady voltage (1.65V) at the node A.

After the integration stage, there is steady and hold stage. That has been imple-

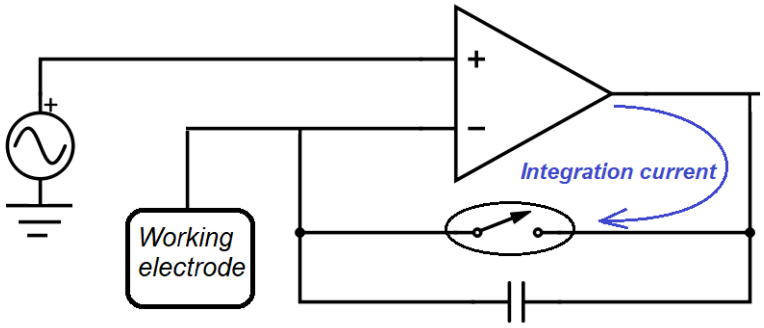

Figure 3.5: Addition of controling switch.

mented with the topology at Fig. 3.6. According to that, the voltage at node A remains steady and by proper switching timing the charge injecting is canceled and there is only a steady offset [22].

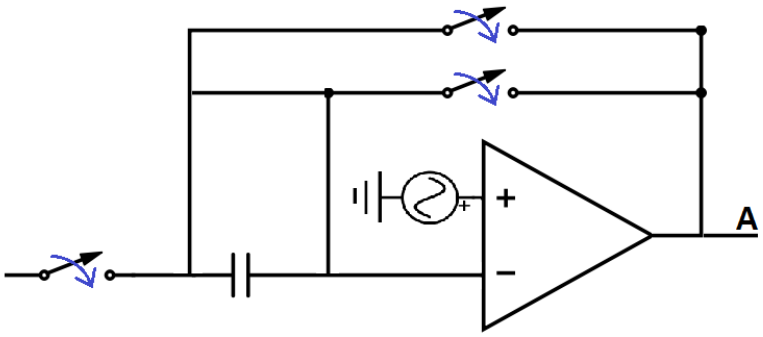

Figure 3.6: Steady and Hold stage.

3.3 The disadvantages of the Topology

Firstly, the two-stage amplifier could not buffer efficiently the voltage at node A Fig. 3.2 for high currents. More specific, for high measured currents there was a voltage drop at node A. Furthermore, the two-stage differential amplifier suffers from stability issues [23].

The second pole of a two-stage differential amplifier is

$$f_2 = \frac{G_m}{2\pi C_L} \tag{3.1}$$

Where the capacitance of the equation is the load capacitance. So when two-stage differential amplifiers drives a big load then the frequency of the second pole idecreases and the phase margin decreases too. In order to compensate for that the compensation capacitance Cc Fig. 3.3 needs to be increased. At the specific project, the driving load is big and the purpose of the design is to be functional for even bigger loads. So, the two stage amplifier is inadequate.

3.4 Managing instability

The instability issues had to been fixed without the increment of the compensation capacitance. The reason is firstly because the trade-off between area and stability indicates that the area should be increased a lot to have a reliable phase margin and secondly even an increased compensation capacitance could not guarantee that the amplifier would remain stable if the load at the working electrode had an increment. Taken into consideration the aforementioned issues, another amplifier has been chosen for the integration stage. That is a one stage folded cascade amplifier Fig. 3.7.

Folded cascode has been chosen as it provides high gain and can ensure stability for big loads. The dominant pole of the folded cascode differential amplifier is

$$f_1 = \frac{1}{2\pi C_L R} \tag{3.2}$$

So when the load capacitance increases the phase margin increases too. As a result, the amplifier gets steadier for bigger loads. That property makes the folded cascode amplifier much more capable for specific requirements and so it has been chosen for the implementation.

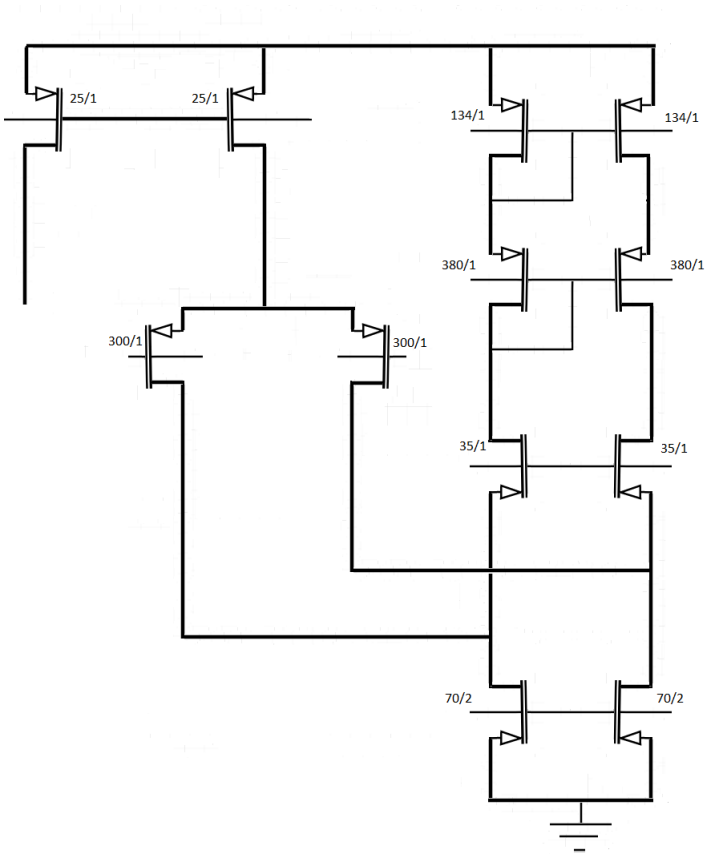

Figure 3.7: Folded cascode differential amplifier.

3.5 Managing voltage drop

As it was previously described, there is an unwanted voltage drop at the node A of the two-stage differential amplifier Fig. 3.2 when high currents were integrated. That voltage drop still exists at the folded cascode topology Fig. 3.7. Therefore, a modification of the sample and hold stage had to take place in order to compensate for that. The new topology that has been derived fixes the problem, providing steady integration, consuming less power and area at same time.

In order to compensate for the voltage drop a new technique has been derived. That can be seen at the Fig. 3.8. Generally there are two stages at the integration process. At the first stage the integration takes place at the two capacitances. At the second stage the capacitance C2 is isolated from the upper part of the circuit and the voltage at the

left plate is defined again by a reference voltage source at 1.65 V. As a result the voltage at the right node increases too. The result is that now the voltage at the right plate of the capacitance has the value similar to the one that it would have if the integration had happened without voltage drop at node A. At the next chapter a much more detailed discription of the design will take place.

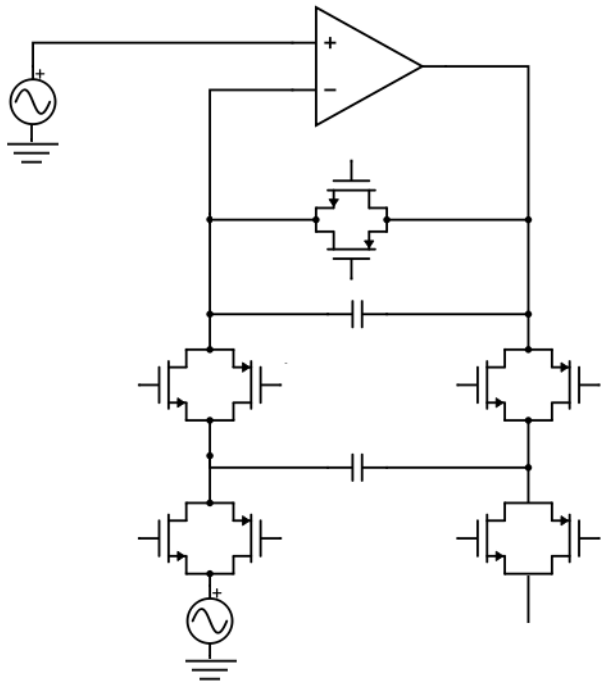

Figure 3.8: New archtecture.

3.6 Chapter summary

This chapter decribes the inital architecture that has been derived. That is an integration tpology and a sample and hold topology.The integration topology integrates the read-out current for a certain amount of time and the sample and hold provides steady output for a certain amount of time. After that are pointed out the limitations of these implementations in terms of stability and measurment range. Finaly, are introduced solutions which deal with these limitations.These sloutions compose a new circuitry which is explained in detain in the next chaplter.

Chapter 4

Analogue circuit

4.1 The integrator

IT was previously explained why a differential folded cascoded amplifier has been chosen for the integration phase. The folded cascode that has been used can be seen at Fig. 4.1. Also at Table 4.1 are presented the main characteristics of the specific amplifier. As it can be seen there is a sufficient phase margin when the whole load is connected to the output of the amplifier. Also, from Fig. 4.1 can be seen that there have been used very large transistors for the input pair and for the current mirror. The reason is that it is crucial for the integrator to integrate linearly and not be influenced by noise or mismatch. By setting these two pair big enough the noise and the mismatch are limited. Furthermore, the integrator needs to be very flexible in order to be able to provide a big range of currents. A restricting issue according to that is the fact that for the extreme cases (highest integrating currents) some transistors might stop operating at the saturation region. In order to deal with that issue the sizing has been chosen so all the transistors are deep in saturation region and it is impossible to change operation region for the range of currents needed.

4.2 The switch

The topology of the integration on and off switch had to be chosen very carefully. The requirements for the switch were that it had to be big in order limit the voltage drop.

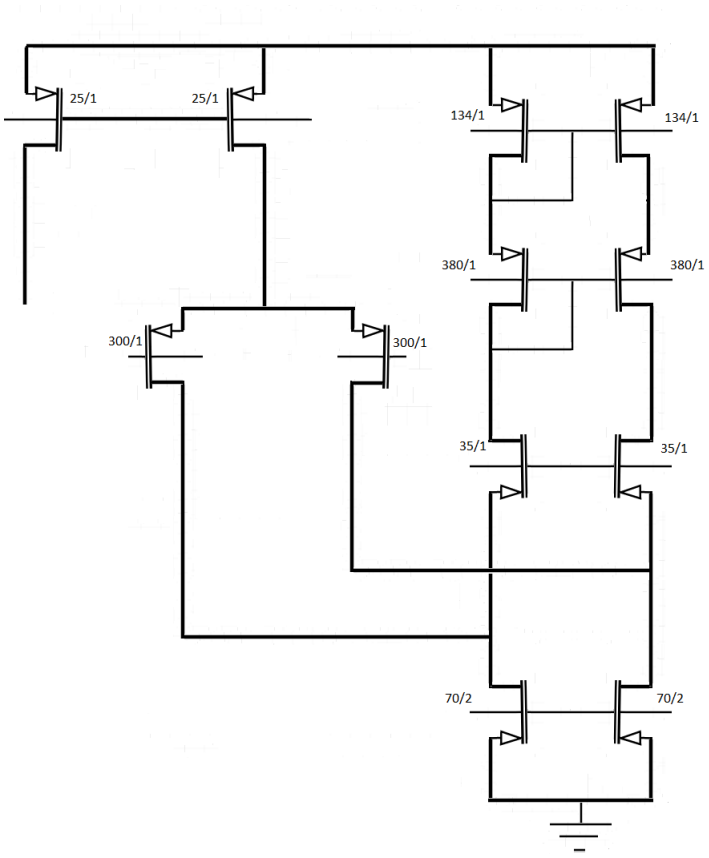

Figure 4.1: Folded cascode differential amplifier.

Parameter	folded cascode amplifier
Gain(dB)	80.2
-3dB bandwidth(kHz)	7.9
Phase Margin (load Capacitance 10nF)	67
Power consumption(mW)	3.12
CMRR(dB)	117.2
Output current(uA)	100

Table 4.1: Specifications of folded cascode amplifier designed.

At the same time the charge injection should be limited as an injected charge on the capacitance would change the amount of charge collected at the integration phase and it would reduce the accuracy of the measurements. The topology that has been chosen is the complimentary switch. Fig. 4.2 [22]. The complimentary switch is useful as with proper sizing it will operate as a resistance when it is closed [22]. The equivalent resistance of

the complimentary switch is

$$R_{eq} = \frac{1}{m_n C_{ox}(W/L)_N(V_{DD} - V_{THN})[m_n C_{ox}(W/L)_N - m_p C_{ox}(W/L)_P]Vin - m_p C_{ox}(W/L)_P} \tag{4.1}$$

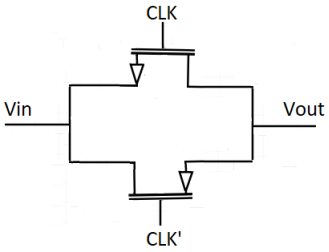

Figure 4.2: The complimentary switch.

According to that, if

$$m_n C_{ox}(W/L)_N = m_p C_{ox}(W/L)_P \tag{4.2}$$

then the equivalent resistance is independent of the input level.

Also, the complimentary switch is ideal for cancelling charge injection [22] . More specific, the effect of charge injection can be limited by the complementary switch as when the switch is turned off the PMOS and NMOS inject opposite charges which cancel each other.

4.3 Sample and Hold and Voltage offset correnction circuit

The current integrated to the right plate of the capacitance creates a voltage that should be sampled and holded. Furthermore there is an offset that should be added to that voltage because, as it was explained at Chapter 2, the integration does not always take place with the left plate of the capacitance fixed at 1.65V. More specific, big currents tent

to cause a voltage drop at the left plate and the integration does not start always from the same point. At Fig. 4.3 it can be clearly seen that the integration starts from 1.56V and 1.643V for currents 100uA and 15uA respectively instead of 1.65 V.

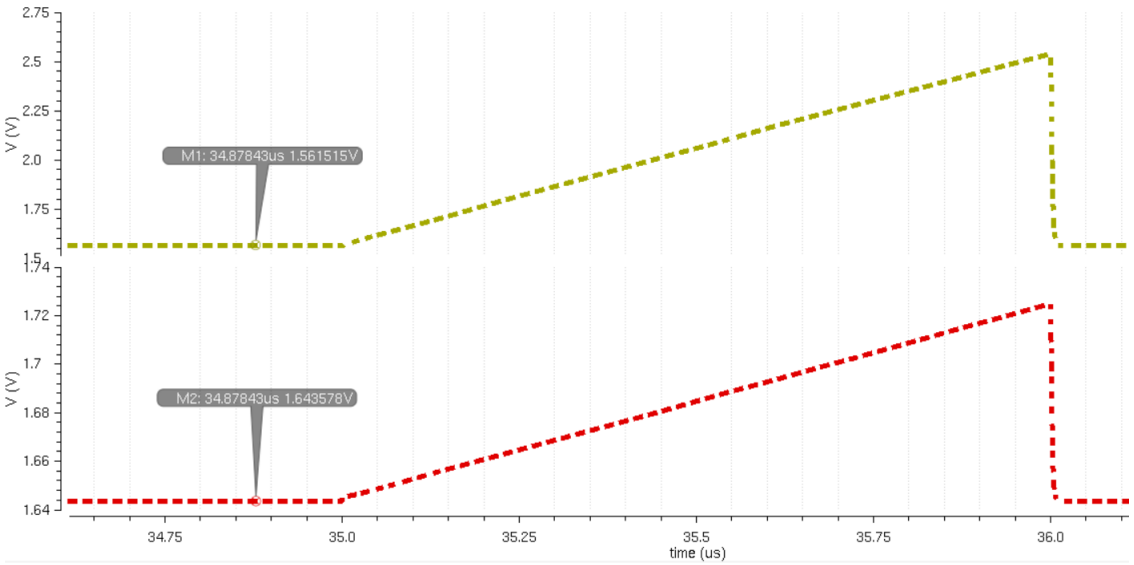

Figure 4.3: Voltage drop for big currents.

The circuitry that has been implemented Fig. 4.4 manages to isolate the voltage after the integration. Then it fixes the voltage drop by adding an offset and after that it holds the fixed value for the hold phase.

4.4 Switch Timing

As it ca be seen from Fig. 4.4 there are 5 different switches that turn on and off different parts of the circuit. These switches separate the integration, sample hold and fixing process into five different phases. The timing of these switches is presented at Fig. 4.5

4.4.1 Phase one : Integration

At the phase one the switch F1 is open and the switches F2 is closed. As a result, during that phase the circuit is like Fig. 4.6. During that phase is when the actual integration onto the two capacitances takes place.

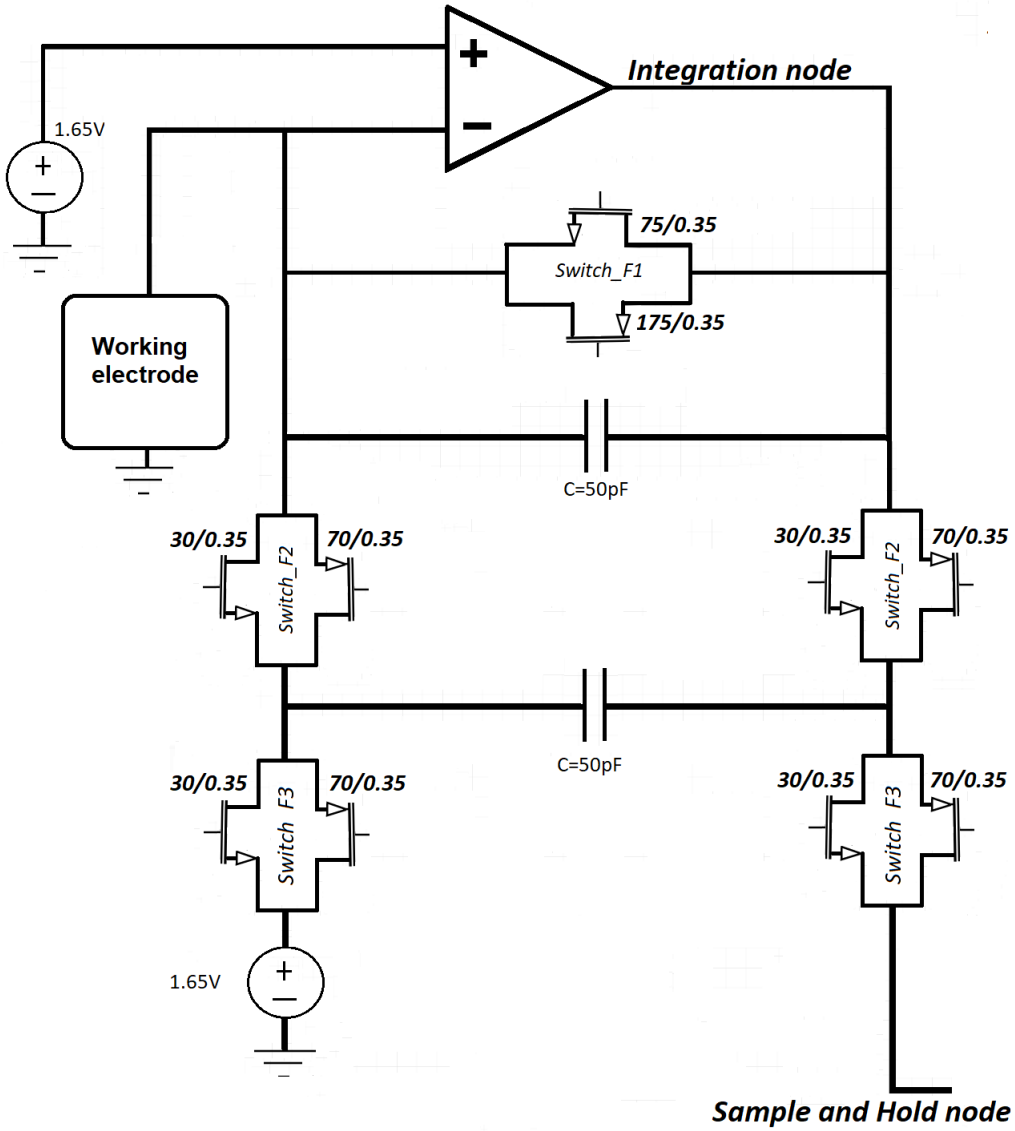

Figure 4.4: Offset correction circuitry.

4.4.2 Phase two : Circuit separation

At phase two 4.9. the switch F1 closes and as a result the current flows through the switch F1 and it is not integrated onto the capacitance. At the same time the switches F2 open and that splits the circuit into two different circuits.

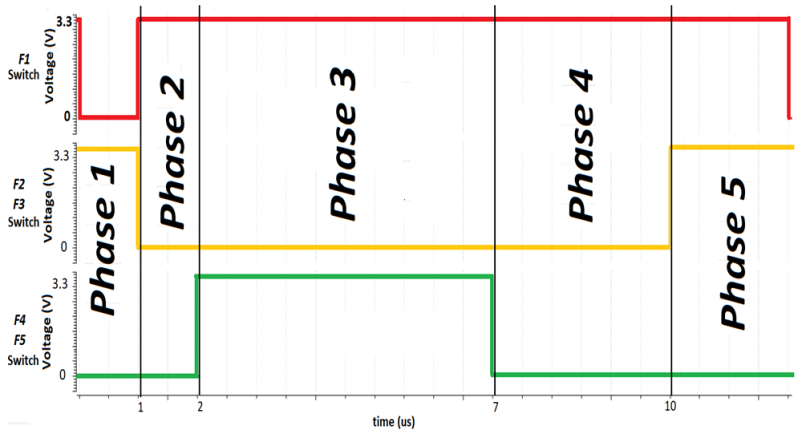

Figure 4.5: Switches timing.

4.4.3 Phase three : Offset correction and hold

At phase three the switches F3 closes. Now the left plate of the capacitance has 1.65V. As a result the voltage at the right plate of the capacitance C2 gets increased by the amount needed in order for the charge at the right plate to has as a reference the 1.65V Fig. 4.8.

4.4.4 Phase four : Offset correction settling

At phase four the switches F3 opens again Fig. 4.9. The duration of that phase is very small but it is very important to exist as it lets the circuit to settle for a small period of time before the reconnection phase.

4.4.5 Phase five : Circuit reconnection

At phase five the switches F2 close again. Now the circuit is connected again and is ready to start the integration phase (phase one) when the switch F1 opens Fig. 4.10.

4.5 Example of the operation of the circuit described

At this section is presented an example of the circuit operation with the switches described at the previous section. The graph presented below indicates how the integration node and sample and hold node Fig. 4.4 operate during those phases. At this graph is pointed

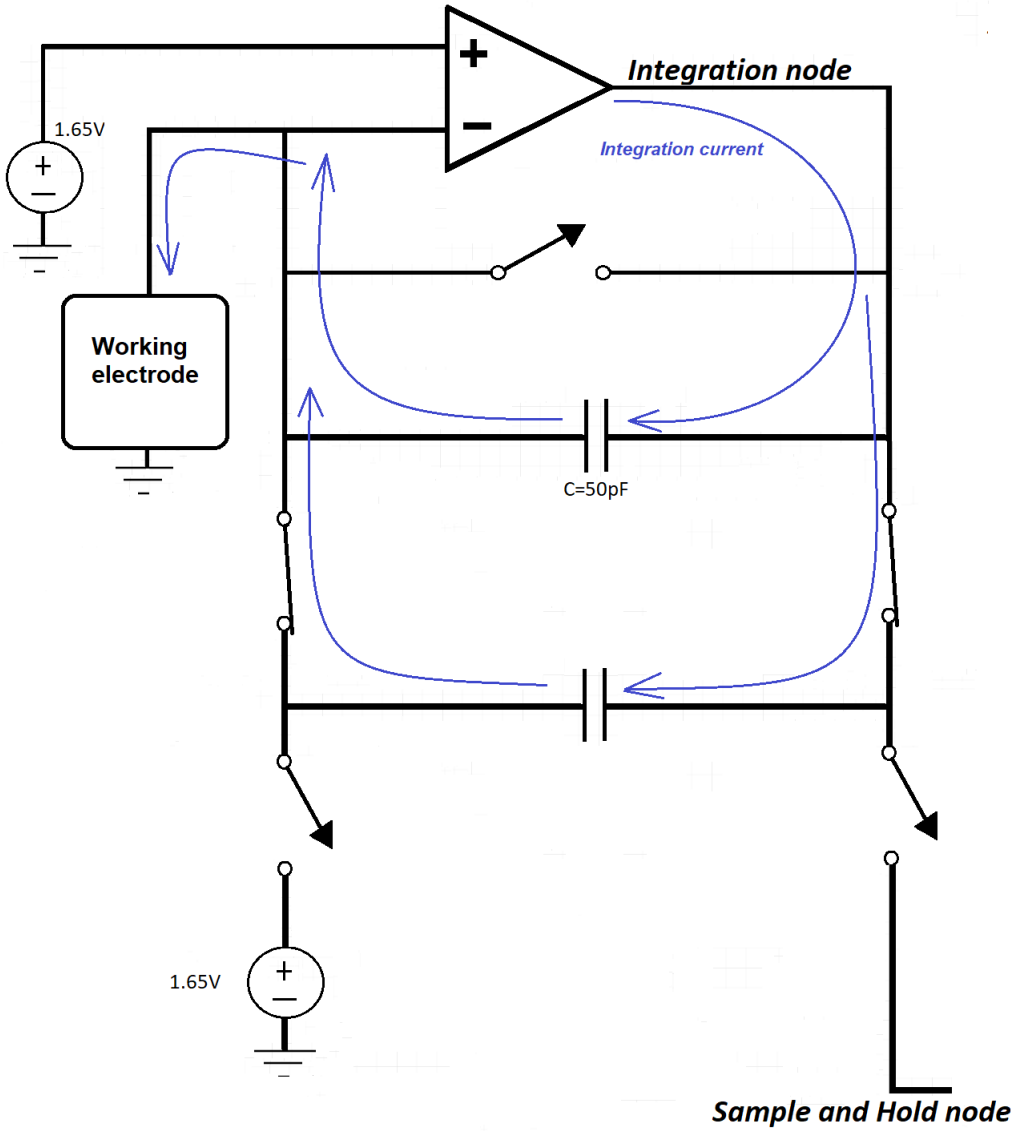

Figure 4.6: Phase one : Integration.

out the importance of offset fixing technique. As it can be seen from Fig. 4.11, the current is big enough to cause a voltage drop and so the integration does not start from 1.65 but from a lower value. During the Offset correction and hold phase (phase three), the holded value its fixed by adding the proper offset. At Fig. 4.11 the integrating current is big (100uA). As it can be seen from the Fig. 4.11 the inegration starts from 1.561V instead of 1.65V. So there is a 89mV offset. The current integrated creates a voltage 2.524V at integration node. However that value needs to be increase by 89mV. That happens at

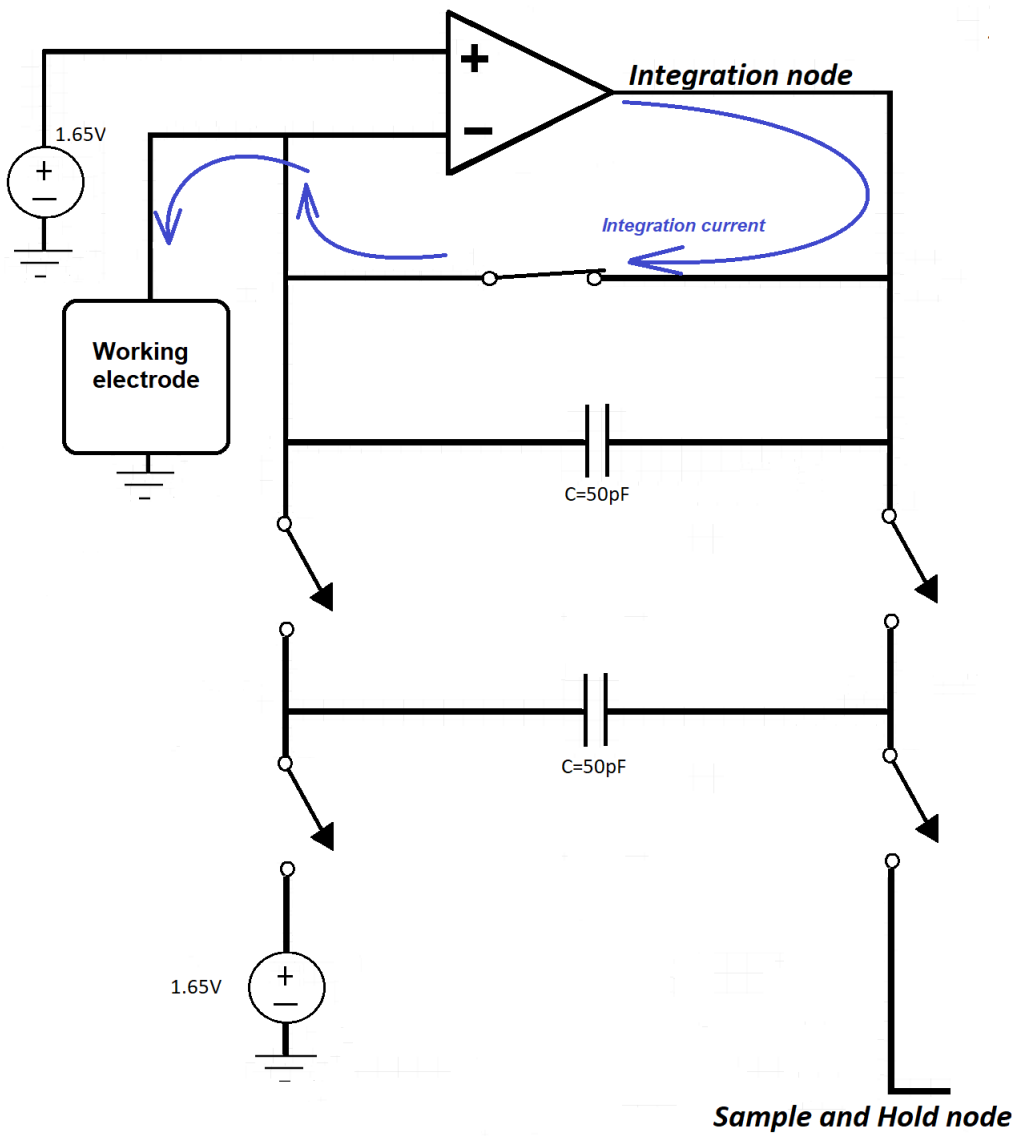

Figure 4.7: Phase two : Circuit separation.

phase three where the holded value is 2.611V whcich is the 2.524V increased by 89mV. By that technique the integration always takes place with reference 1.65V no matter the voltage drop at the integration node due to big currents.

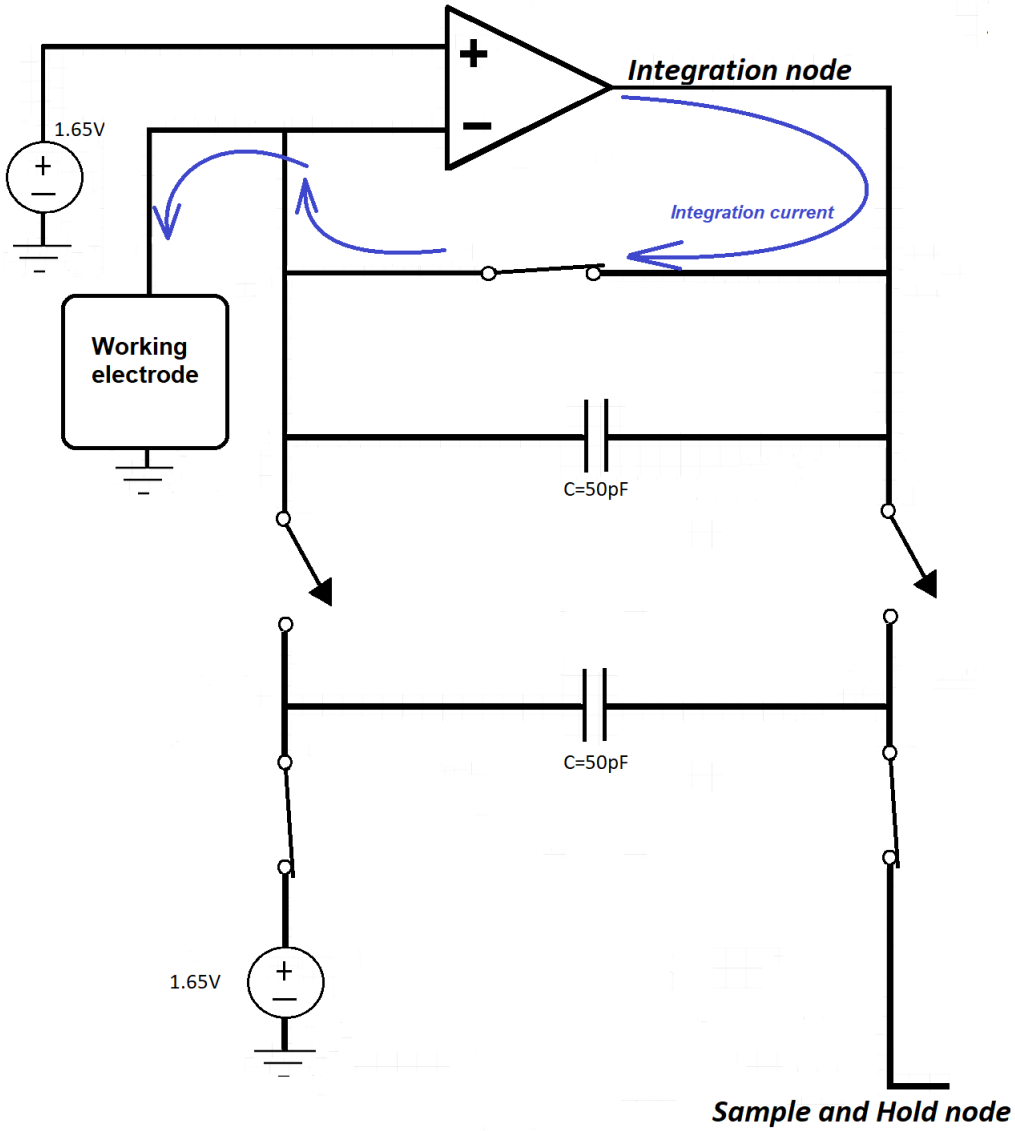

Figure 4.8: Phase three : Offset correction and hold.

4.6 Analogue to Digital Converter

The addition of an Analog to Digital converter is needed to provide a digital output proportional to the current measured. More specific, the results at the Sample and Hold node at phase three Fig. 4.4, Fig. 4.11 are provided at an 8 bit ADC which transforms the measured voltage to a digital 8 bit output. That can be seen at Fig. 4.12.

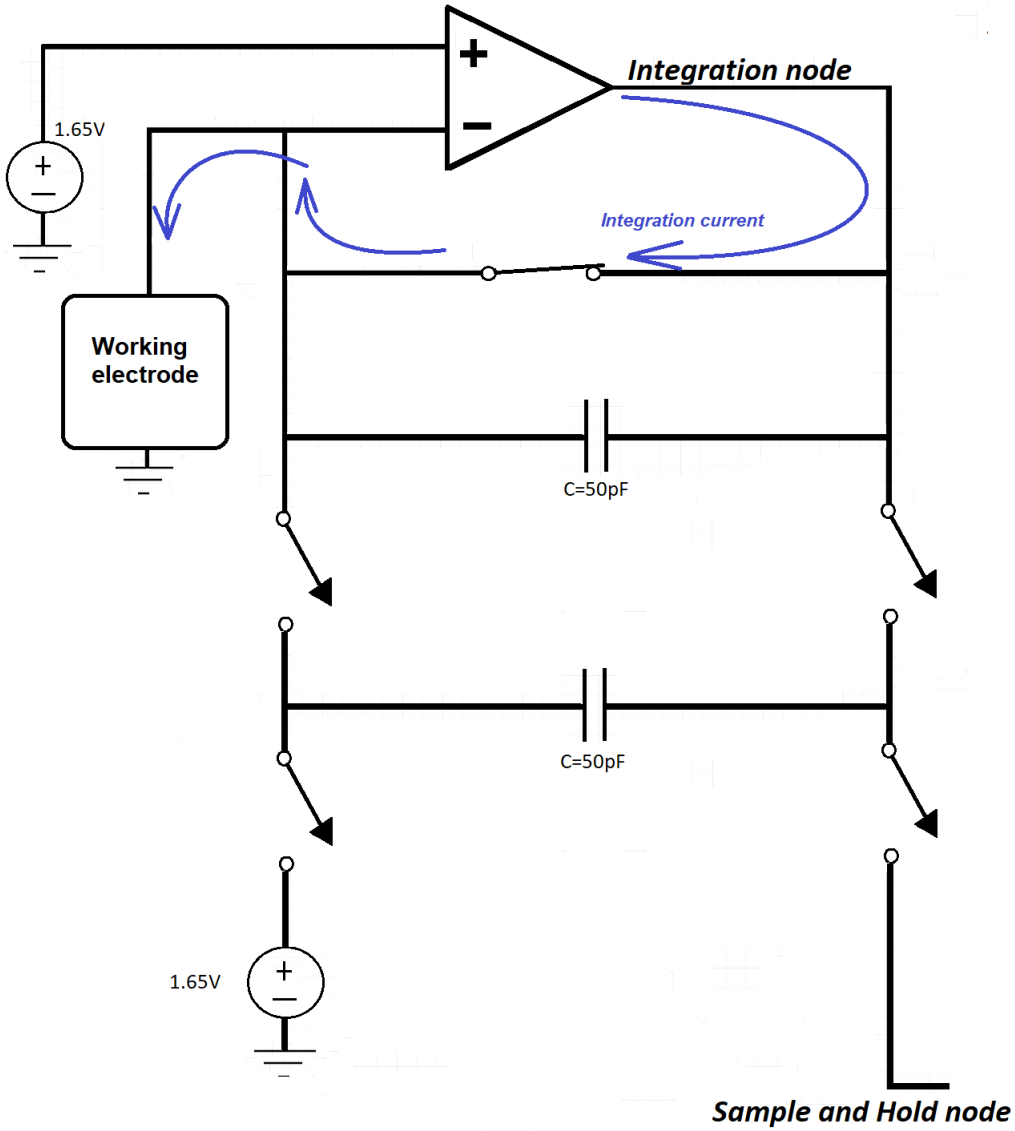

Figure 4.9: Phase four : Offset correction settling.

4.7 Chapter summary

At chapter 4 the topolgy derived at Chapter 3 is explained in detail. More specific, the Analogue readout circuit is described. The new tchnique is analyzed and there is a step by step reprasentation of the different phases. Furthermore there is a description of the switches used and justifications for the specific choice. Moreover is presented the timing managment of the switches of the circuit. In the end there is an example where the

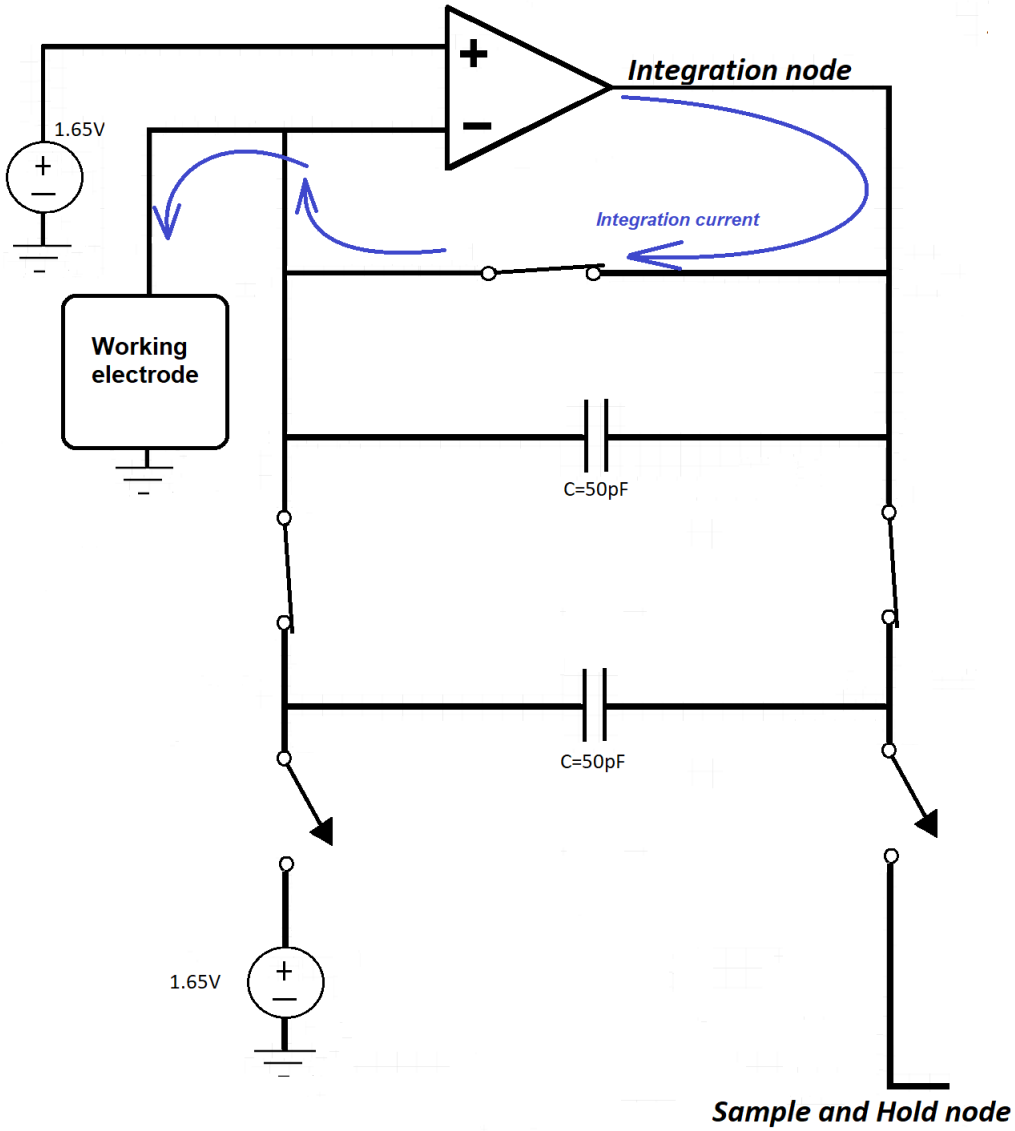

Figure 4.10: Phase five : Circuit reconnection.

integration and hold node are monitored during the whole phases which points out the importance of each phase and prooves the efficiency of the derived technique.

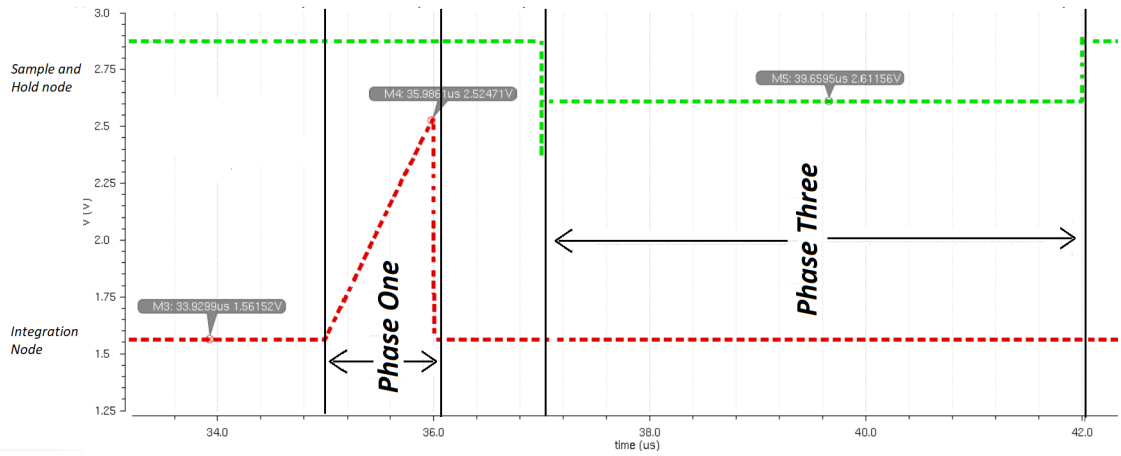

Figure 4.11: integration fixing example.

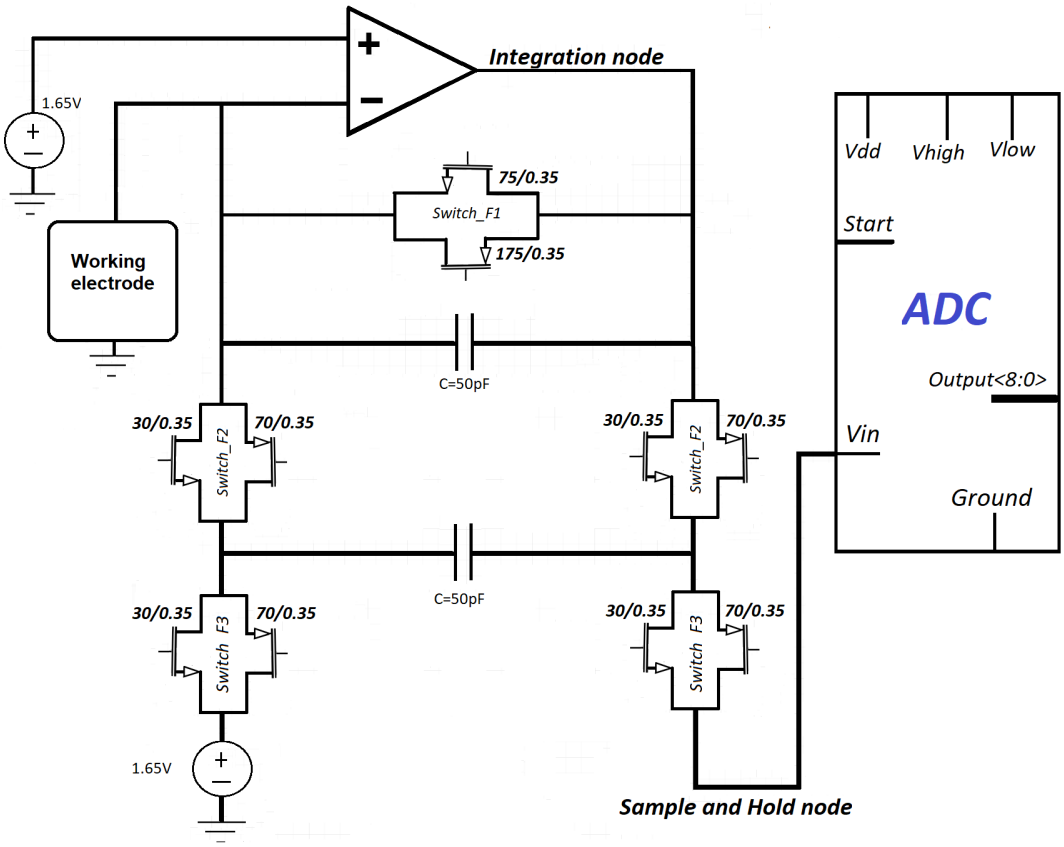

Figure 4.12: Circuit with ADC.

Chapter 5

Digital Circuit-Range Expansion

5.1 Range limitations

TH e circuit described at chapter 4 is being optimized is terms of area, power consumption and linear integration performance. However, there is a limitation. That is that the circuit can measure only a very small range of currents in accuracy. More specific, the circuit can measure currents from 4uA to 100uA but for smaller currents the integration is insignificant. That becomes clear at Fig. 5.1. Here are presented an integration for 10uA and one for 750nA. As it can be noticed, the integration at 750 nA is insignificant as it is only 1.656V. So it is only 6mV higher that the reference which is 1.65V and therefore does not contain any useful information and it cannot be interpreted by the ADC as it is too small.

Given that the designed chip targets to a wide range of currents, some of them much smaller than 750nA, it is clear that a modification should take place. The main idea is to modify the integration time for different ranges of currents. By doing that, there will be an accurate scale for each current range which will maintain reliability of measurements for the ADC.

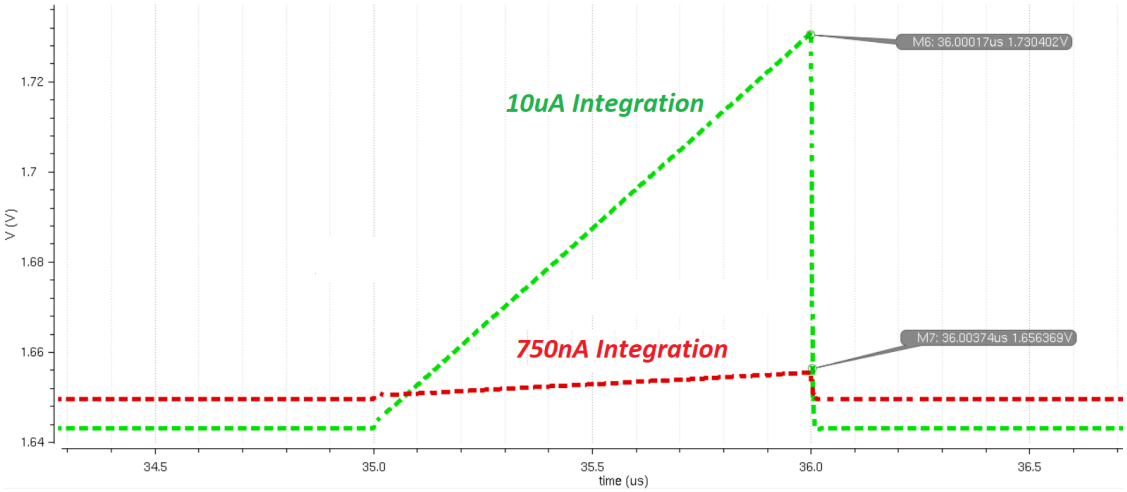

Figure 5.1: Folded cascode differential amplifier.

5.2 Proposed solution

The concept of the proposed solution can become clearer from the Fig. 5.2. Here, the measurement A measures a current 2uA using a frequency while the measurement B measures the same current with a lower frequency. As it can be seen, at the first frequency the current does not get integrated for enough time to give a suficiently big value as it gives only 1.67V. However when the intgration of the same current takes place with the second frequency it provides a voltage big enough for measurments which is 2.47V. The concept can easily be expanded to more frequencies. So, for example if the measuring current is 300 fA then even the second scale is insufficient and another even lower measuring frequency is needed in order to achieve a well-defined measurement.

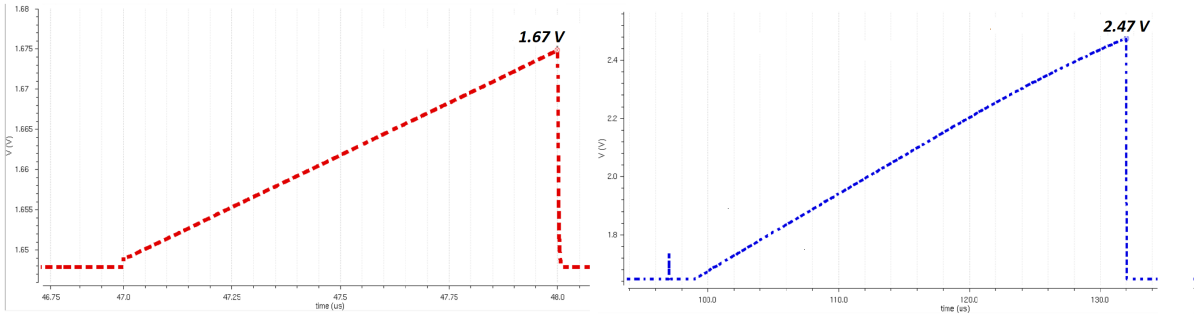

Figure 5.2: Integration for the same current with two different frequencies.

So the solution proposed is an addition of a circuit as a feedback loop. That circuit will have two tasks. Firstly, it will have to decide if the operating frequency is the proper one. Secondly it will have to provide the correct frequency in order the integrator-sample and hold circuit to use that frequency as integration time for a well-defined measurement.

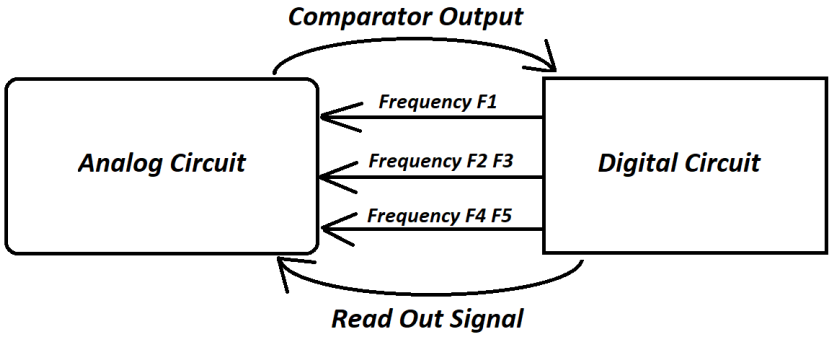

Figure 5.3: Analog and digital circuit interaction.

Fig. 5.3 is a qualitative description of the circuit with the feedback loop. The Analogue block consists of the already described integrator, the sample and hold but it has also a comparator. That comparator has as input the output of the sample and hold node. The analogue circuit can be seen at Fig. 5.4 .

The comparator compares the measured voltage with a threshold (1.68V). If the measured voltage is bellow that threshold then the comparators output is equal to one. If the measured voltage is bigger than the threshold the comparators output is equal to zero. Those one and zero are interpreted properly by the feedback block. If the feedback block receives a one that means that the measured voltage is too small and therefore the integration frequency needs to be reduced. If the feedback block receives a zero that means that the integration time is the suitable one for the specific current. It becomes clear from the description of the feedback block that this needs to be a digital block.

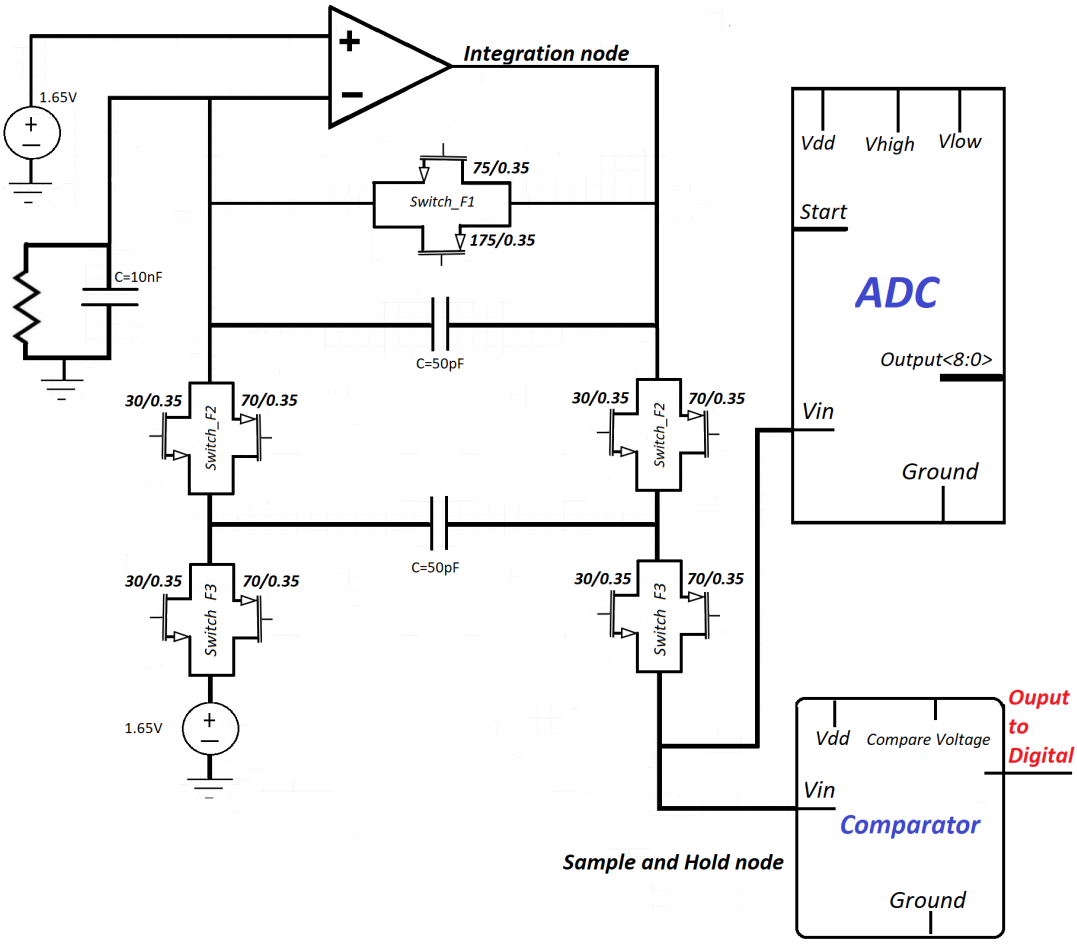

Figure 5.4: Analog with ADC and Comparator.

5.3 The digital block

The digital block is the right block at Fig. 5.3. It has as input the output of the comparator from the analogue block. When it receives a one then it needs to provide the next lower frequency in order to increase the integration time. As a result, a new integration takes place. If the new integration does not provide a sufficient voltage value, then the comparator provides a new one at its output and that means that the digital should change again the provided integration frequency to the next lower one.

5.4 Algorithm expansion

Although that algorithm seems sufficient it is not yet. The reason for that is that it does not take into consideration variations at the integrating current that are likely to happen. For example, the integration current could be 600nA and that means that the integration frequency should change from the first to the next lower. But if the measurement takes place when there is a momentary variation at the current then the measured current could be big enough to provide a one at the digital block and so there will be no change at the integrating frequency which is a wrong decision.

In order to confront the previously described weakness of the design the operations of the digital block have been expanded. More specific, the digital block receives 10 comparator outputs measured with the same frequency. Then, only if more than six of them indicate that the frequency needs to be changed it changes the frequency. By doing that it is ensured that the circuit will integrate at lower frequency only if there are very strong signs that this needs to be done.

When the integrating frequency is well defined by the steps described, then that frequency is fixed for the next 10 measurements. The digital block keeps that specific frequency for the next 10 measurements in order to take place 10 correct integrations. The output of the sample and hold node is given to the ADC. The digital block will also provide as an output the specific operating mode. So, at the output there will be a ready signal which informs the user that the results are valid and ready, a Mode signal which will indicate the integrated frequencies that the measurements took place and also the actual measurements from the output of the ADC.

As it can be concluded, there are two phases. The Mode specification phase and the Readout phase. At the Mode specification phase the circuit decides the frequencies that needed to be used for proper measurements. At the Readout phase the circuit provides 10 outputs using the frequencies decided at the Mode specification phase. After the 10 outputs, the circuit restarts again. That can be seen at Fig. 5.5.

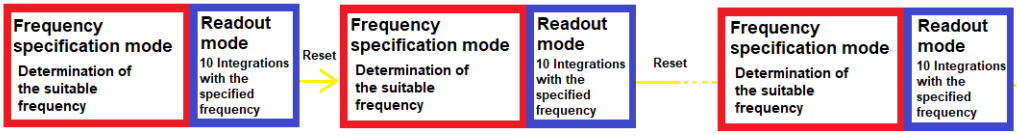

Figure 5.5: The two modes of the digital block.

5.5 Power saving modification

By the description of the algorithm designed it can be seen that the ADC is not used at the Frequency specification phase. Managing to turn the ADC off at the Mode specification phase will be a significant improvement of the power consumption of the whole circuit. The reason for that is that the ADC is a power intensive block which consumes and important amount of power if operates continuously. In order to turn the ADC off when it is not needed an extra signal is created by the digital block. That signal is contacted to the start signal of the ADC and allows it to be turned on and off. That new signal is setted to one only when the circuit is at the Readout phase and the sample and hold node has valid data.

5.6 Implementation of the Digital block

The description language chosen for the design of the digital block its VHDL. The code that has been developed is described at Fig. 5.6. What happens is that the circuit firstly identifies the proper operating frequency and after that it provides outputs using that frequency.

5.7 Chapter summary

Chapter 5 describes the Digital block of the topology. Firstly is explained why the topology without digital block is insufficient. The measuring weaknesses are pointed out with examples. After that the alogrithm of the digital block is described. Its main charecteristics are being analyzed and further modifications on the alogirthm are discussed. The

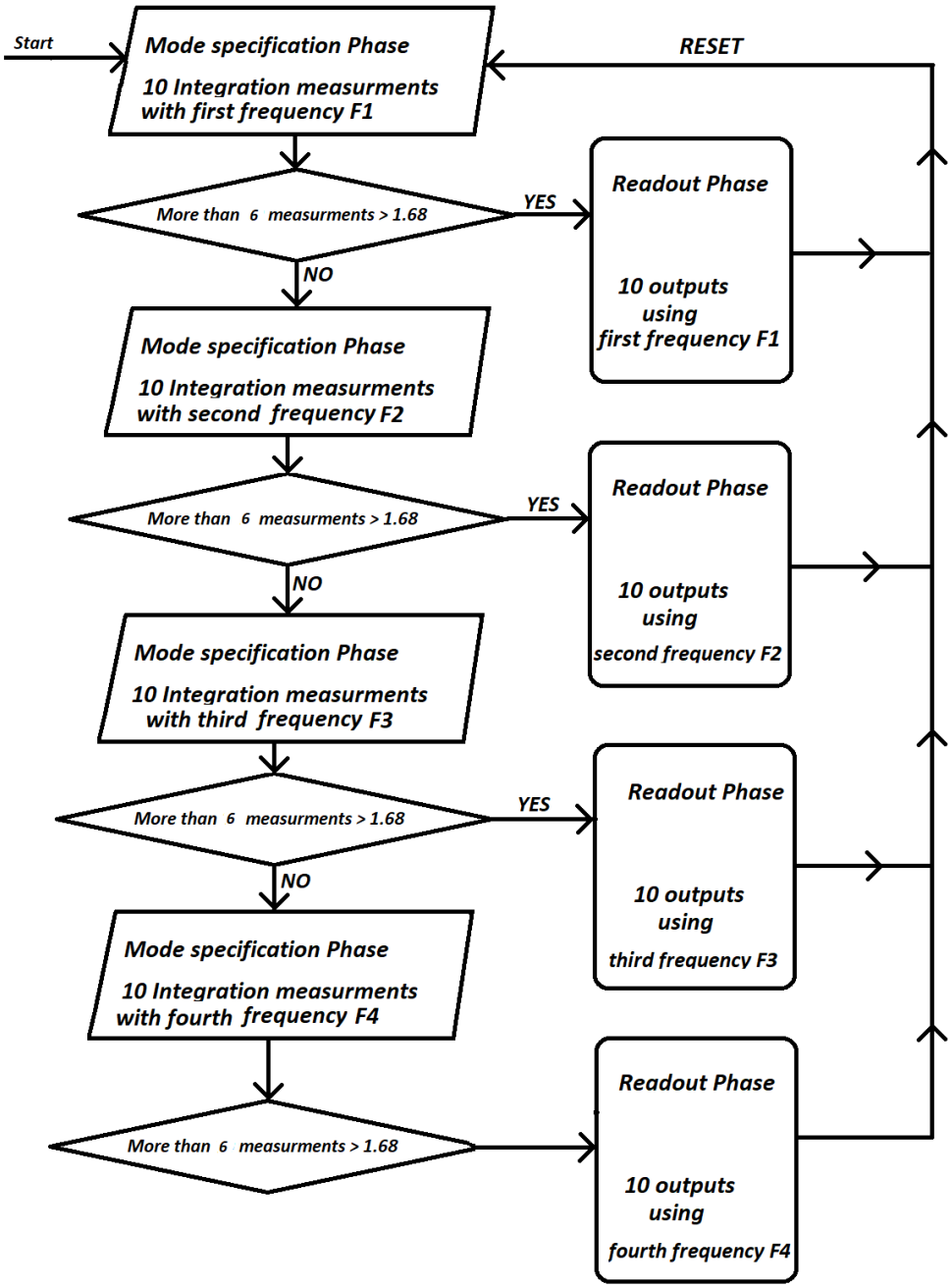

Figure 5.6: The Algorithm.

interaction with the analogue block is also presented.

Chapter 6

Simulated results and final chip

6.1 Final implementation range specifications

TH e implementation designed contains four different measuring scales which measure different ranges of currents. The currents measured at each scale with the respective integration frequency and current noise of each scale are presented at Table 6.1.

Mode	Current Range	Integration Frequency	$I_{inTotal}$
Mode One	100uA - 3.021uA	83kHz	11.2nA
Mode Two	3.021uA - 86.4nA	23kHz	4.5nA
Mode Three	86.4nA - 2.47nA	815Hz	350pA
Mode Four	2.47nA - 86pA	24Hz	6pA

Table 6.1: Current range, frequency and current noise at each scale.

Each of these scales had to be tested separately to confirm that the integrations at the specific scale are linear. Therefore, several simulations took place for each scale. Fig. 6.1 Fig. 6.3 Fig. 6.5 and Fig. 6.7 present how the Voltage of the Sample and Hold node of the analogue part (the voltage provided to the ADC) changes for different measured currents when the integration current flows to the working electrode. Fig. 6.4 and Fig. 6.6 and also and Fig. 6.8 present how the Voltage of the Sample and Hold node of the analogue part (the voltage provided to the ADC) changes for different measured currents when the integration current flows to the working electrode.

Fig. 6.6

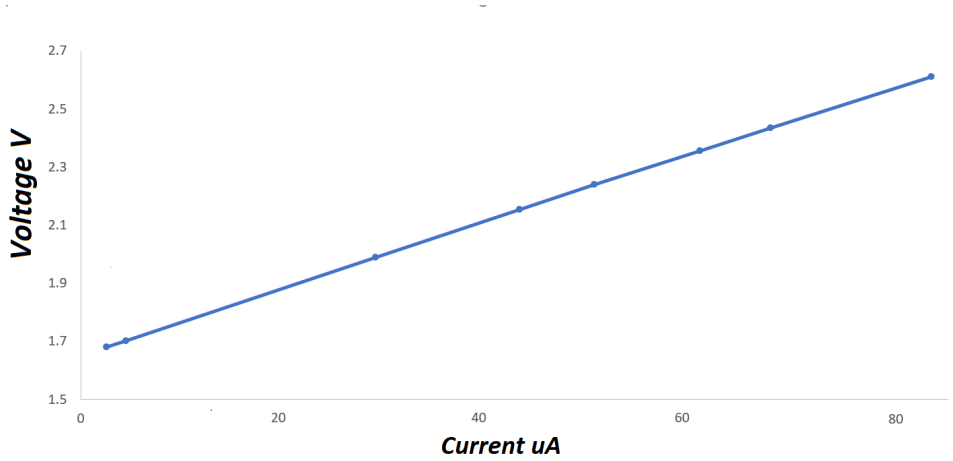

Figure 6.1: First Mode. Direction of the integration current: To the working electrode.

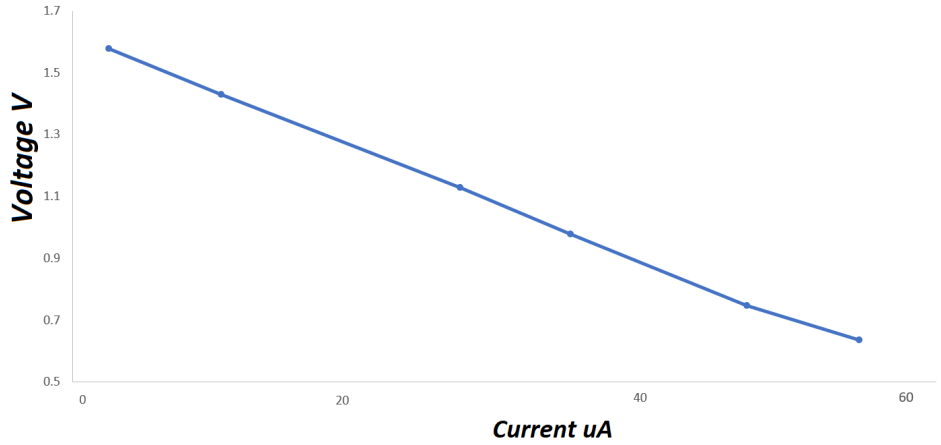

Figure 6.2: First Mode. Direction of the integration current: From the working electrode.

6.2 Whole system simulations

In order to ensure the proper functionality of the whole system, full system simulations took place Fig. 6.9. The target was to ensure the proper interaction between the analogue block and the digital block because checking the functionally of them separately could not guarantee the functionally of the whole system. A simulation for the measurement of a very small current is took place. The current measured was 53nA so the system had to adjust and reduce the frequency twice to generate the suitable measuring frequencies.

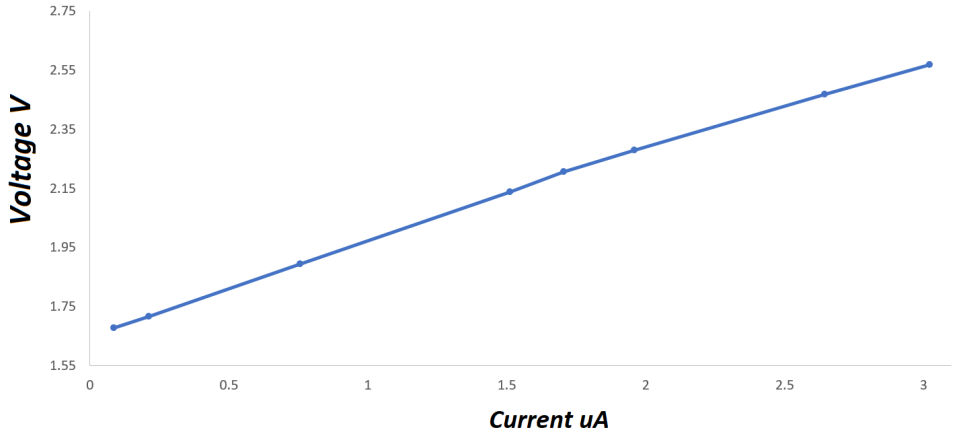

Figure 6.3: Second Mode. Direction of the integration current: To the working electrode.

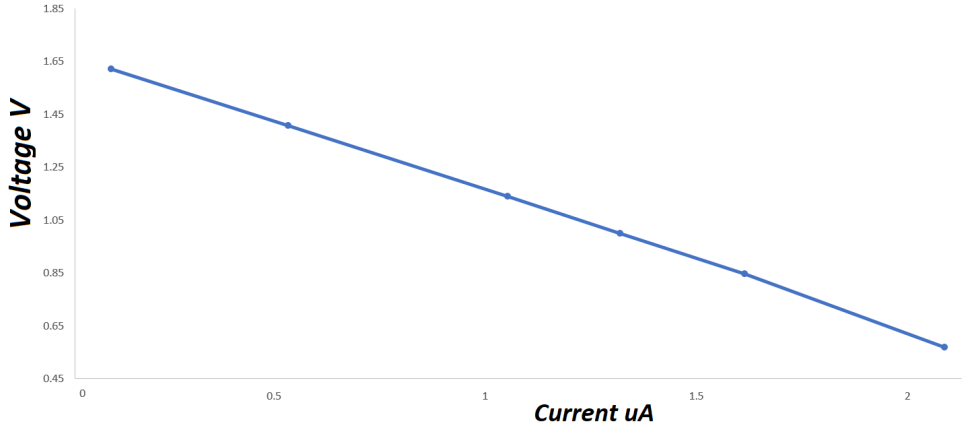

Figure 6.4: Second Mode. Direction of the integration current: From the working electrode.

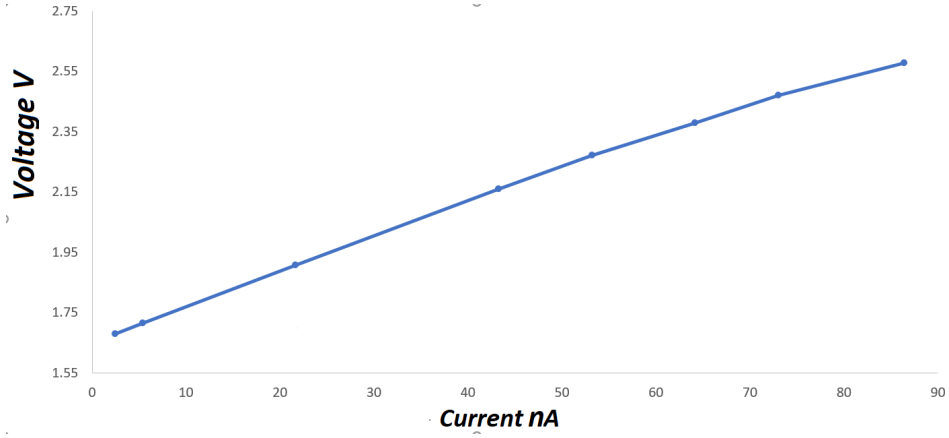

Figure 6.5: Third Mode. Direction of the integration current: To the working electrode.

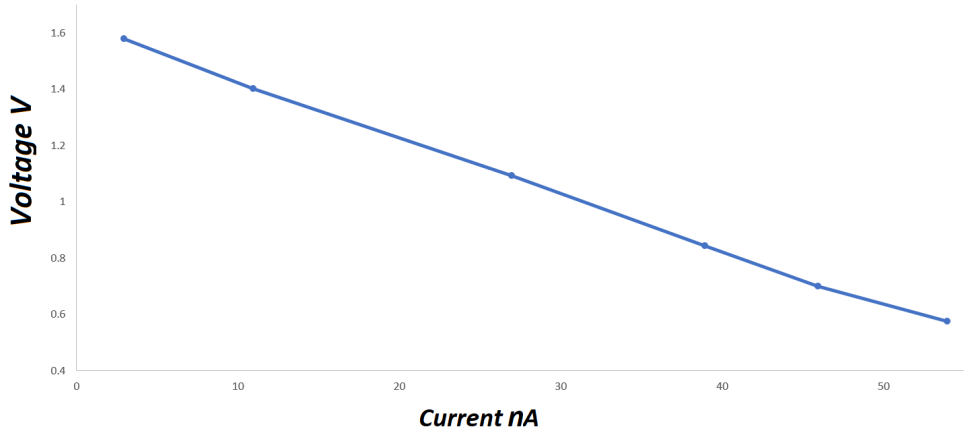

Figure 6.6: Third Mode. Direction of the integration current: From the working electrode.

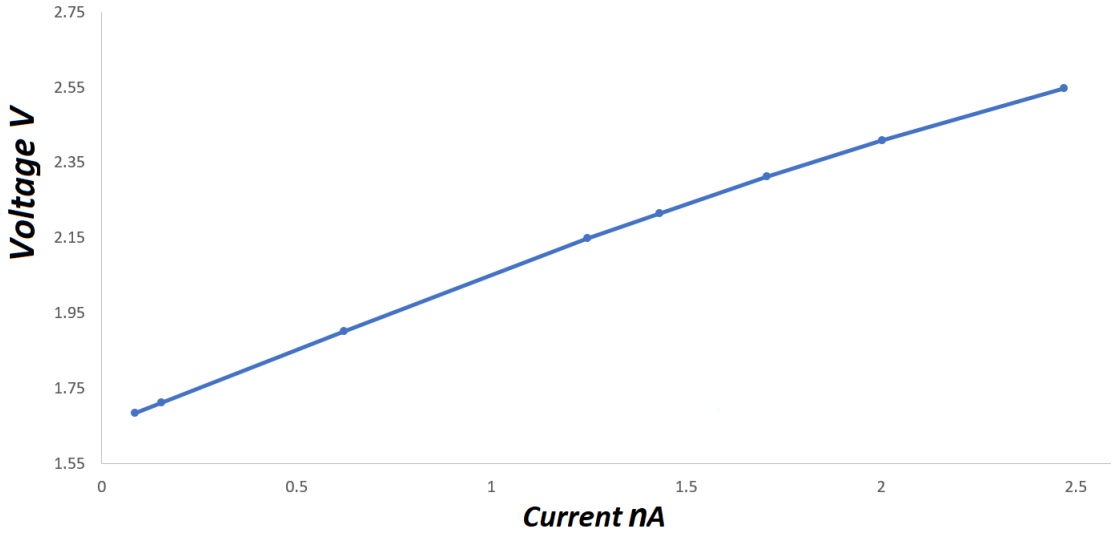

Figure 6.7: Fourth Mode. Direction of the integration current: To the working electrode.

Fig. 6.10 presents the clock signals for the first scale. As it can be seen, the integration lasts for 2us. The integration time of the first mode is not enough to integrate a sufficient amount of charge. The comparator detects that the integrated current creates a very small voltage rise. So the Sample and Hold node Fig. 6.9 has a smaller value than 1.678 V and therefore the Decision signal becomes one and the comparator sends a logic one to the digital block. This means that the analogue block informs the digital block that the integration time needs to be increased. However, at the graph the integration time remains the same for the next measurement. That happens because, as it has been explained, the digital block does not change integration frequency just because one measurement indicates

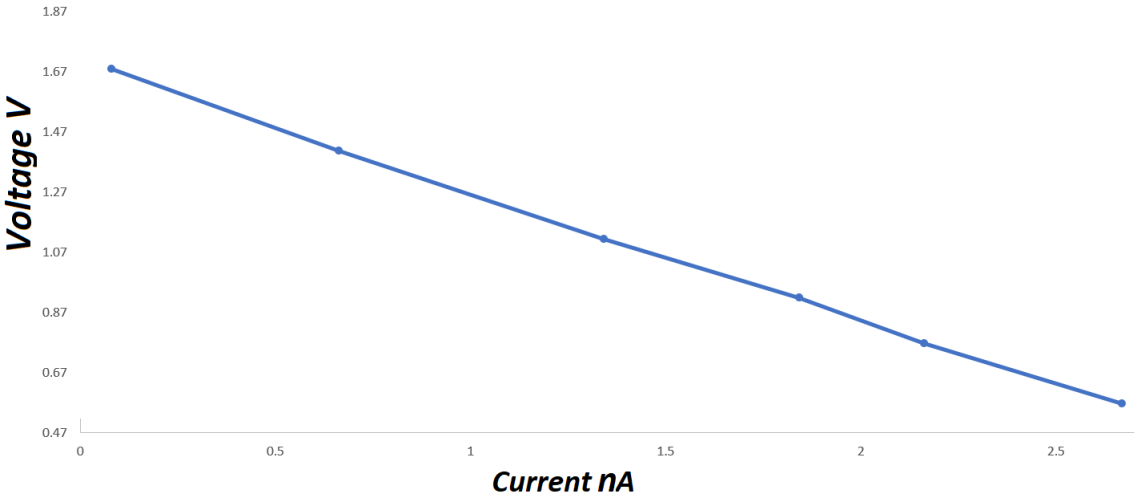

Figure 6.8: Fourth Mode. Direction of the integration current: From the working electrode.

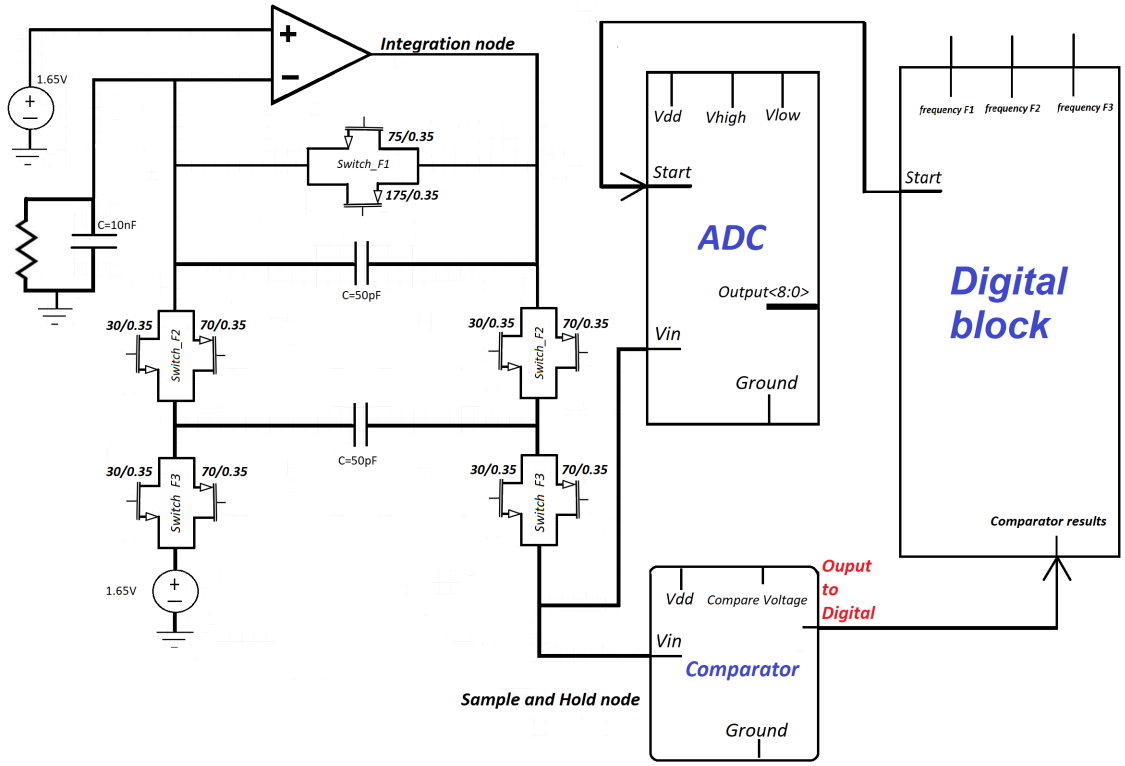

Figure 6.9: Whole system test.

it but it should receive at least 6 logics ones out of 10 measurements. During all that time the Start signal remains to logic zero as the operating frequency has not been specified yet so the ADC cannot start operating.

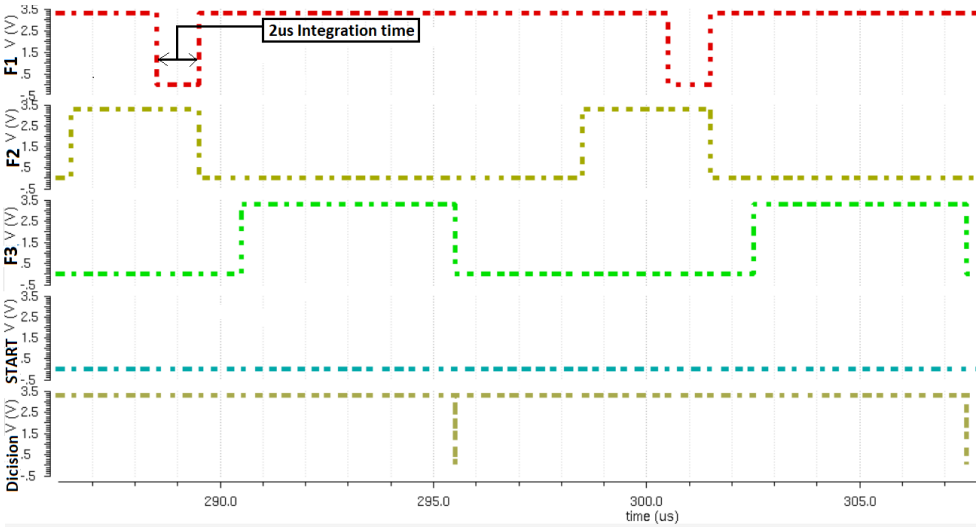

Figure 6.10: First Mode.

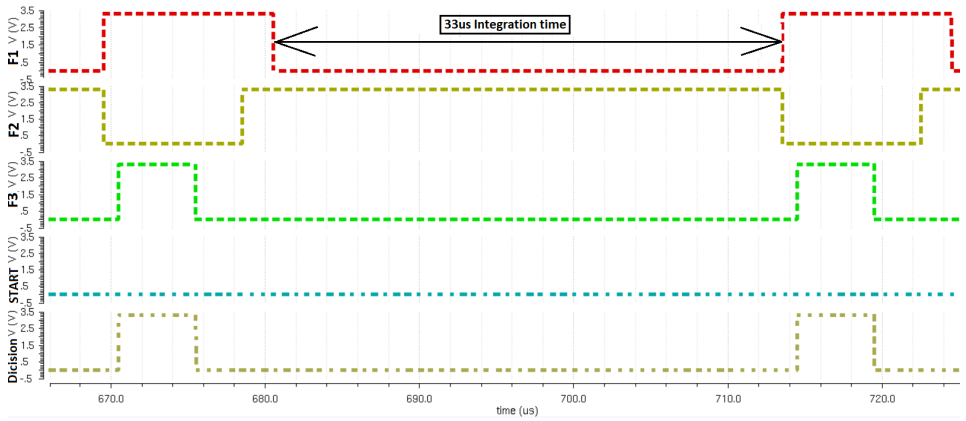

Figure 6.11: Second Mode.

Fig. 6.11 presents the new frequencies that the digital block generates. It can be seen that the integration time has been increased to 33us. However, the signal Decision of the comparator remains one for every measurement again. That means that even the new integration time is not sufficient enough to provide a detectable measurement. So, the frequencies of the switches need to be changed again. Furthermore the Start signal continues to remain to logic zero as the operating frequency has not been specified yet so the ADC can not start operating.

At Fig. 6.12 are presented the switching timings for the third mode. The Decision signal is constantly zero. That means that the integration time is sufficient enough. How-

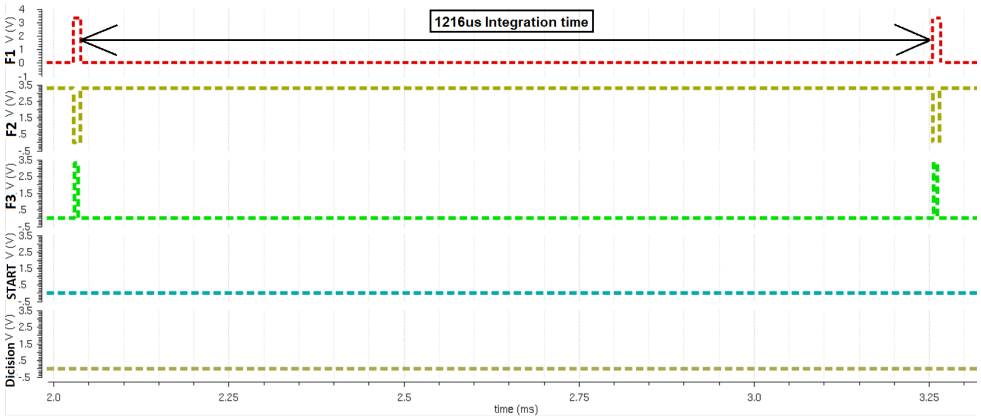

Figure 6.12: Third Mode.

ever, the digital block needs to receive at least six out of ten indications that the frequency is the proper one, thats why ten integrations take place. When the ten integrations are completed and the switching frequencies are well defined, then the signal Start of the digital block becomes logic one. That turns on the ADC at the analogue part and the digital part goes to the readout phase. Here 10 current integrations take place with the defined frequency but now the ADC is turned on.

Fig. 6.13 shows the voltage at the integration node during the whole process. As it can be seen at the first and second integration frequencies the integration is negligible. However, with the third frequency a suitable integration takes place. Fig. 6.14 presents how the ADC output corresponds to the integrations. Initially it can be seen the Frequency specification phase where integrations take place in order for the suitable integration frequency to be specified. After 10 integrations using the first frequency and 10 integrations using the second frequency Fig. 6.13 there are 10 integrations with the third frequency which is the proper one. The decision signal remains constantly zero for the 10 integrations with the third frequency and that means that the digital block should start the Readout phase where for 10 integrations the ADC is turned on and in has as input the output of the Sample and hold node. At Fig. 6.14 when the ready signal is high that means that the outputs of the ADC are valid. As it can be seen for the output of the ADC is 1101 0101 which corresponds to 2.466 V integration voltage.

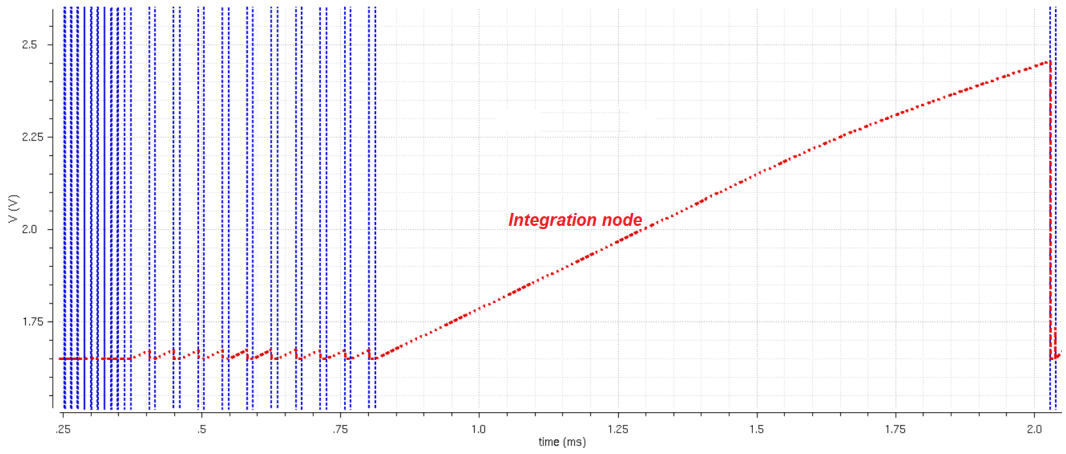

Figure 6.13: The integration node.

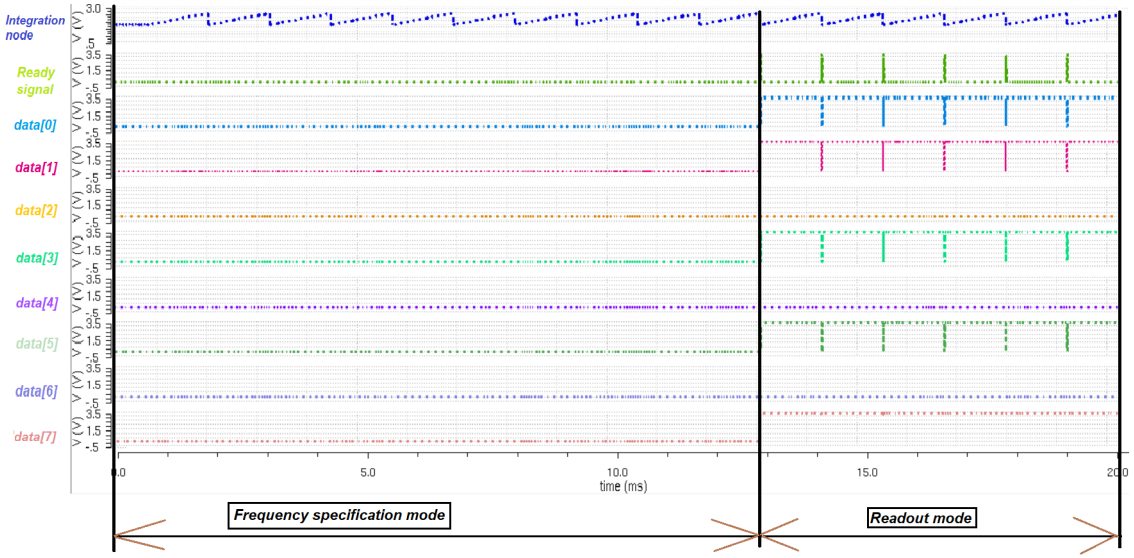

Figure 6.14: The integration node.

6.3 Monte carlo simulations

Monte carlo simulations took place for the critical nodes of the topology that define the stability and the homogeneity of the results. These nodes are the Integration node and the Sample and Hold node at Fig. 6.9. After completing monte carlo simulations for a big number of samples a new problem emerged. The problem was that for almost the one third of the experiments there was an unexpected voltage drop at the Integration and Sample and Hold node. In order to track the cause of that problem more monte calro

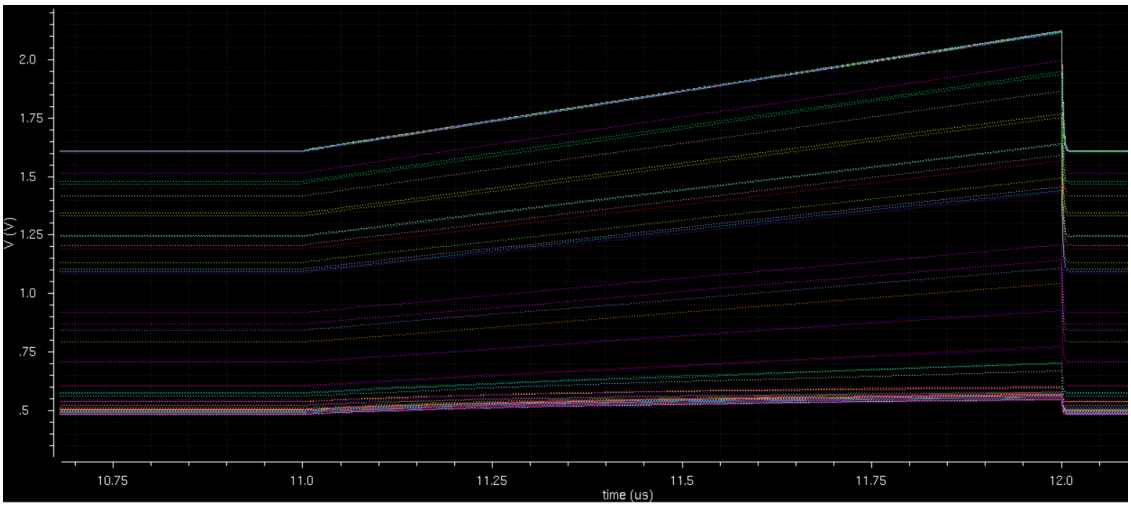

Figure 6.15: Integration node before the voltage bias change.

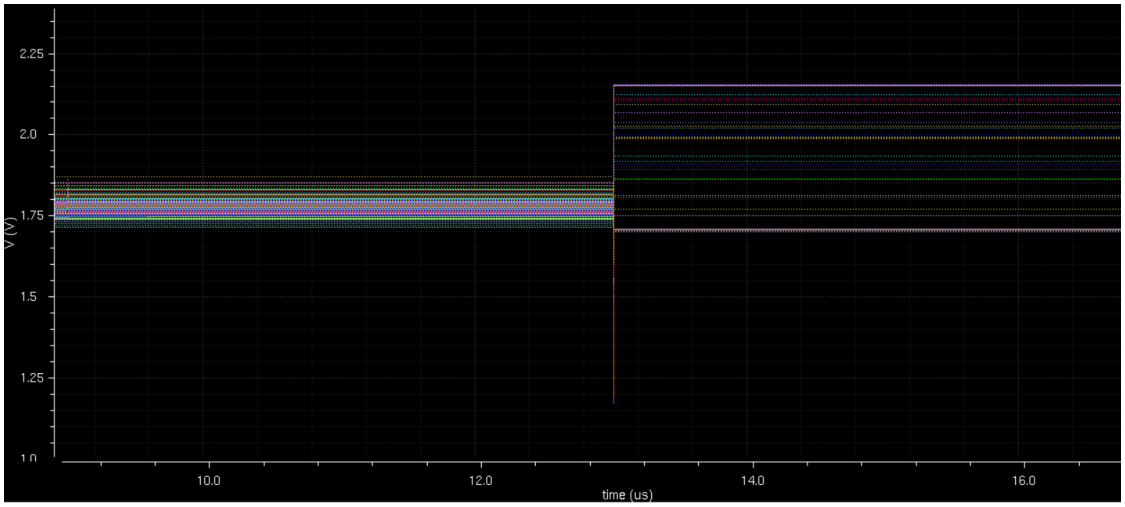

Figure 6.16: Sample and Hold node before the voltage bias change.

simulations took place excluding specific parts of the topology each time in order to define which part was causing that unexpected drops. It turned out that the folded cascode amplifier was causing the problem. More specific at the simulation where the nmos pairs of the folded cascode amplifier where excluded the results were significantly better. So it has been concluded that the nmos pairs where not deeply enough in the saturation region and therefore for some variations at the monte carlo simulation there were entering the triode region. The result of that was unexpected voltage drop at the Integration node. Change the bias voltage a little drag the nmos pair deeper in the saturation region and

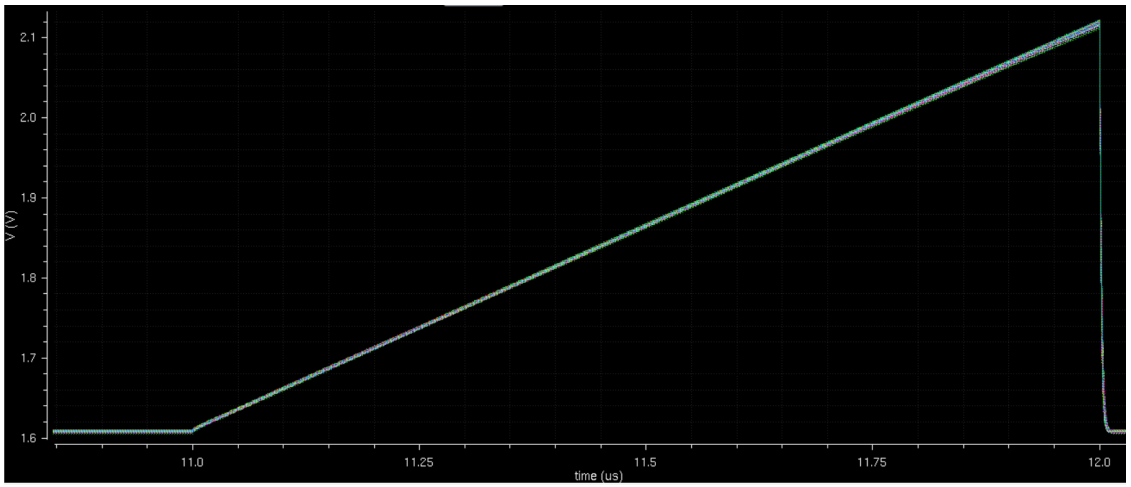

Figure 6.17: Integration node after the voltage bias change.

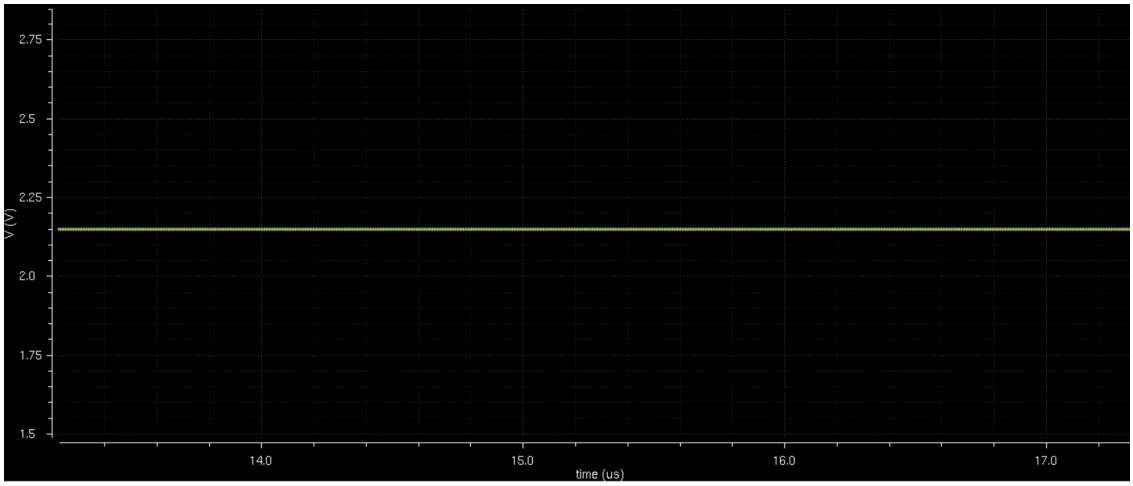

Figure 6.18: Sample and Hold node after the voltage bias change.

that led to significantly better monte carlo results. That can be seen clearly at Fig. 6.15, Fig. 6.16, Fig. 6.17, Fig. 6.18 . At Fig. 6.15, Fig. 6.16 it can be seen the voltage of the Integration node and the Sample and Hold node before the change at the bias voltage. At Fig. 6.17, Fig. 6.18 it can be seen the voltage of the Integration node and the Sample and Hold node when the bias voltage has changed in order to drive the nmos pair deep in the saturation region. The variations at Fig. 6.17, Fig. 6.18 are negligible whereas the respective variations at the Fig. 6.15 are clearly unacceptable.

6.4 Noise

The total input-referred current noise $I^2_{inTotal}$ determines the minimum detectable current, therefore it should be computed for each mode. Initially the relationship between the input current noise I^2_{in} and the voltage noise at the input of the ADC (Sample and hold node) V^2_{out} should be determined Fig. 6.9. That is

$$V_{out} = \int_0^{T_{clk}} \frac{I_{in}}{C} dt \tag{6.1}$$

$$= \frac{T_{clk} I_{in}}{C} \tag{6.2}$$

so,

$$I^2_{inTotal} = (\frac{T_{clk}}{C})^2 V^2_{out} \tag{6.3}$$

The V^2_{out} is measured using noise simulation. Therefore, from the equation 6.2 there are 4 different $I^2_{inTotal}$, one for each mode. These $I^2_{inTotal}$ can be seen at Table 6.2.

Mode	Integration Frequency	$I_{inTotal}$
Mode One	83kHz	11.2nA
Mode Two	23kHz	4.5nA
Mode Three	815Hz	350pA
Mode Four	24Hz	6pA

Table 6.2: frequency and current noise at each scale.

6.5 Final Layout

Fig. 6.19 and Fig. 6.20 presents the designed layout of the folded cascode amplifier and switches used at the integrator respectively. The input pmos pair is critical as it is the first

stage of the amplifier and so the most important one in terms of noise. Therefore, as it can be seen the input pmos pair is big enough to limit the input noise. Furthermore, localized guard rings have been used at each transistor pair to reduce the substrate noise [24]. Also, the common cetroid technique has been used to the input differential pair as that technique decreases the sensitivity in process variations and mismatch [25]. The switches at Fig. 6.20 are also surrounded by localized guard rings to limit substrate noise.

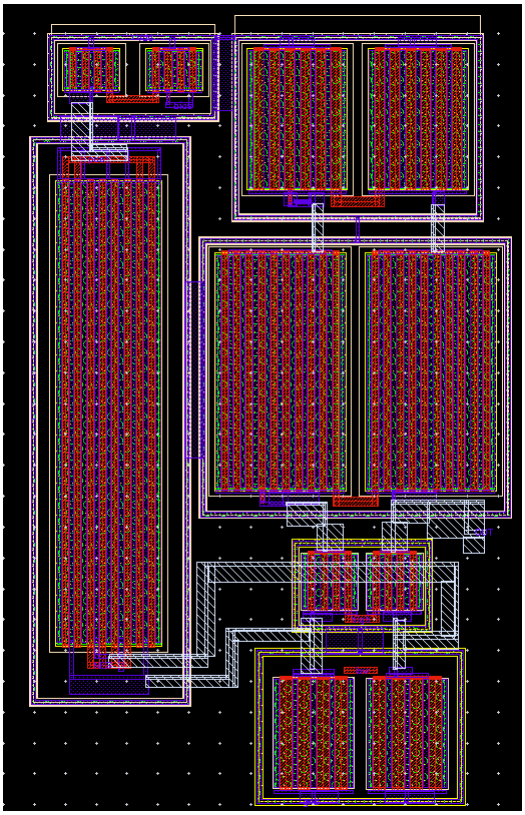

Figure 6.19: The folded cascode layout.

Fig. 6.21 presents the layout of the whole integrator topology. That includes the folded cascode amplifier, the switches and the two integrating capacitances. Post layout simuation took place for the specific topology as it is crusial to see a more realistic behaviour or that part of the circuit. The reason for that is that part of the circuit dictates the accuracy of the measurments. The other parts are and ADC and a Comparator already tested so their behaviour is already known. The Fig. 6.23 shows the results of the postlayout simulation. The voltage of the integration node and the voltage of the sample

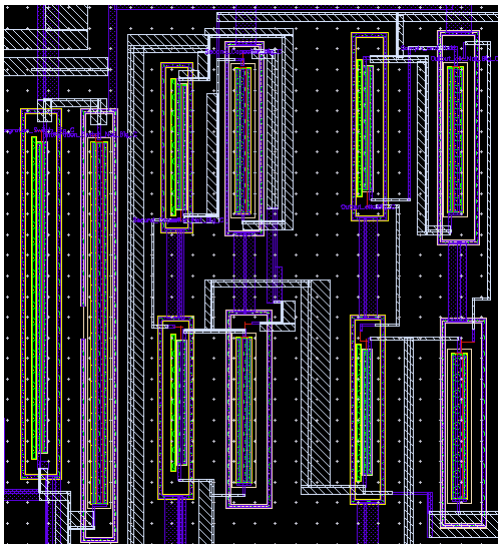

Figure 6.20: The switches of the topology.

and hold node are presented. As it can be seen, the voltage offset correction is not perfetct now. The offset is 86 mV and the voltage added at the offset correction node is not 86 mV but 61 mV.

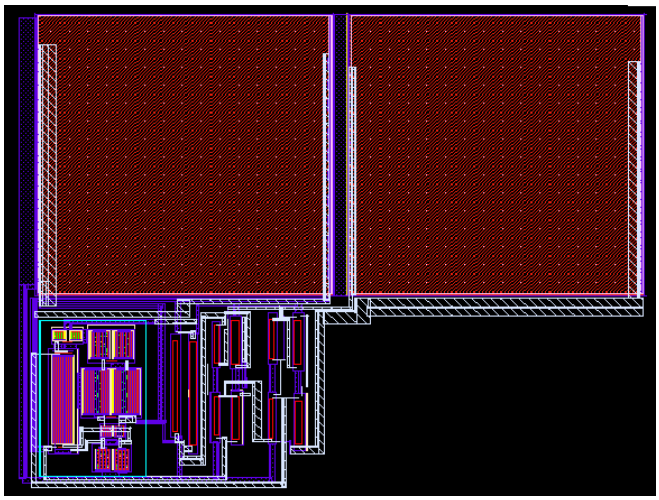

Figure 6.21: The integrator.

Fig. 6.22 presents the layout of the whole system. The most sensitive block is the Integrator and it has been placed as far as possible from the digital block which is causing the most noise.

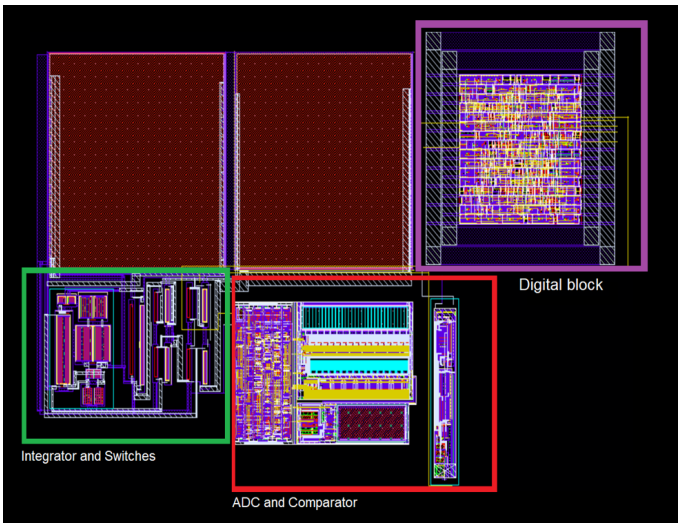

Figure 6.22: The layout of the whole system.

6.6 Postlayout simulation

Post layout simulations took place for the integrator which consists of the folded cascode amplifier, the switches and the two integrating capacitances because it is crucial to see a more realistic behaviour of that part of the circuit. The reason is that this part of the circuit dictates the accuracy of the measurements. Fig. 6.23 shows the results of the postlayout simulation. The integrating current of the simulation is 100uA and that means that the circuit operates wat the first mode Table 6.1. The voltage of the Integration node and the voltage of the Sample and hold node Fig.6.9 are presented. As it can be seen, the voltage at the integration node increases linearly and the voltage is held steady at the sample and hold node. However, the voltage offset correction is not perfect now. The offset is 86 mV and the voltage added at the offset correction node is not 86 mV but 61 mV.

Fig. 6.24 presents the voltage at the integration node for the postlayout simulation. The integrating current of the simulation is 85 nA and that means that the circuit operates at the third modeTable 6.1. As it can be seen there is a small voltage drop at the beginning of the integration which is adding a new offset at the integration process.

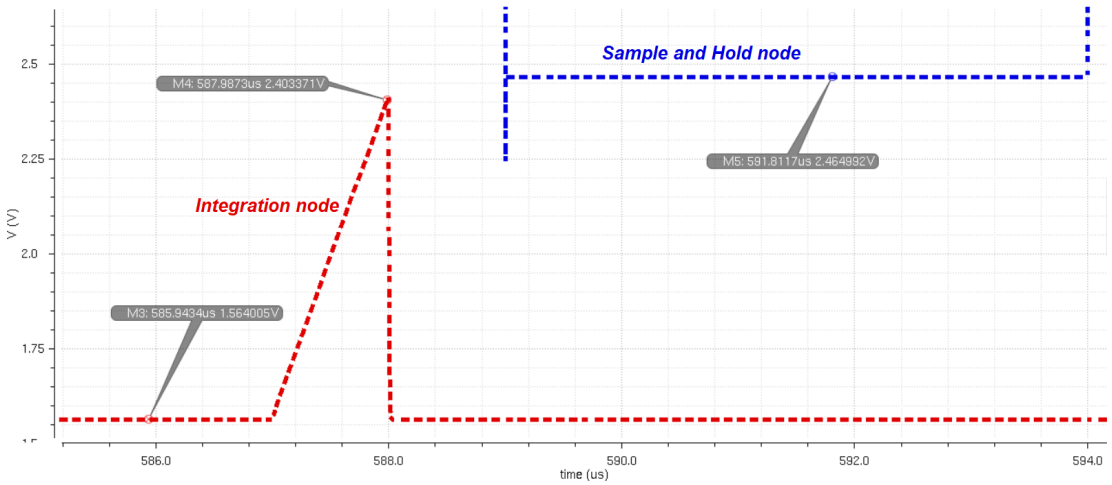

Figure 6.23: Postlayout simulation results of the integration node and the sample and hold node.

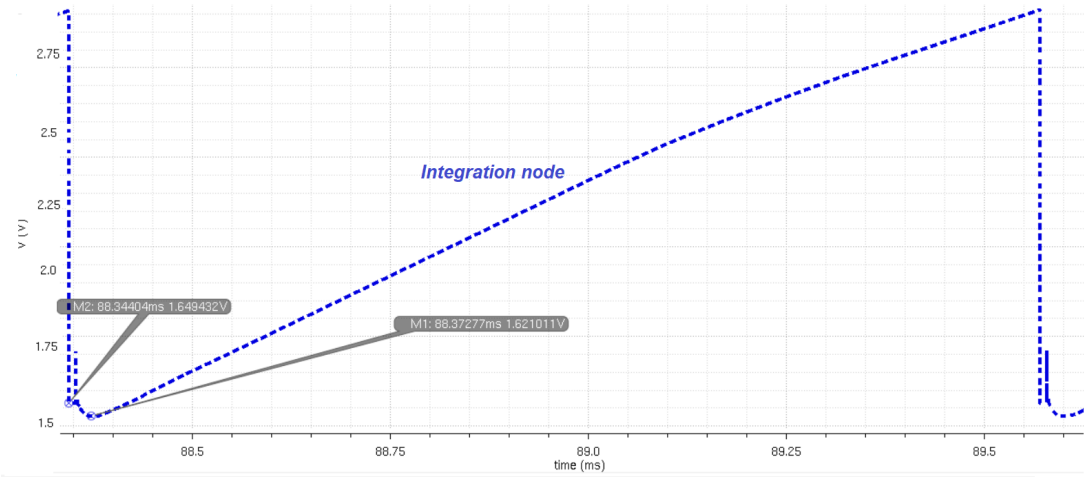

Figure 6.24: Postlayout simulation results of the integration node with an extra offset caused by the parasitic capacitances.

6.7 Chapter summary

Initially are given the specifications of the designed system. The measuring ranges and the respective operating frequencies that have been achieved are presented. Moreover, a full system simulation is described. Detailed explanation of each step of the simulation is described and the interaction between the two main blocks of the design is pointed out. Furthermore, are presented the results of the monte carlo simulations. The weaknesses of the implementation that were discovered during the monte carlo simulations are pointed out and the solution that has been used to solve them is presented. Moreover, is described

the layout of the system and its main figures are explained. Finally, are presented the postlayout simulation of the integrator. The differences that are introduced due to the parasitic capacitances included are pointed out.

In the end in given a final graph which describes and summarizes all the aforementioned topics. More specific, Fig. 6.24 presents clearly the two modes of the design for a small readout current (50nA). The Frequency specification mode and the Readout mode. From Fig. 6.24 can be seen the integrations as the frequencies change from high to lower. As the frequencies change the signal Change frequency is logic one which means that the frequencies need to change again. When the integration time is suitable, signal Change frequency remains at logic zero and the frequencies are stabilized. Now the circuit operates at the Readout mode. There the signal ADC on turns on the ADC when the data at the Sample and hold node are valid and 10 measurements are taken. After that the circuit restart and the same process takes place again.

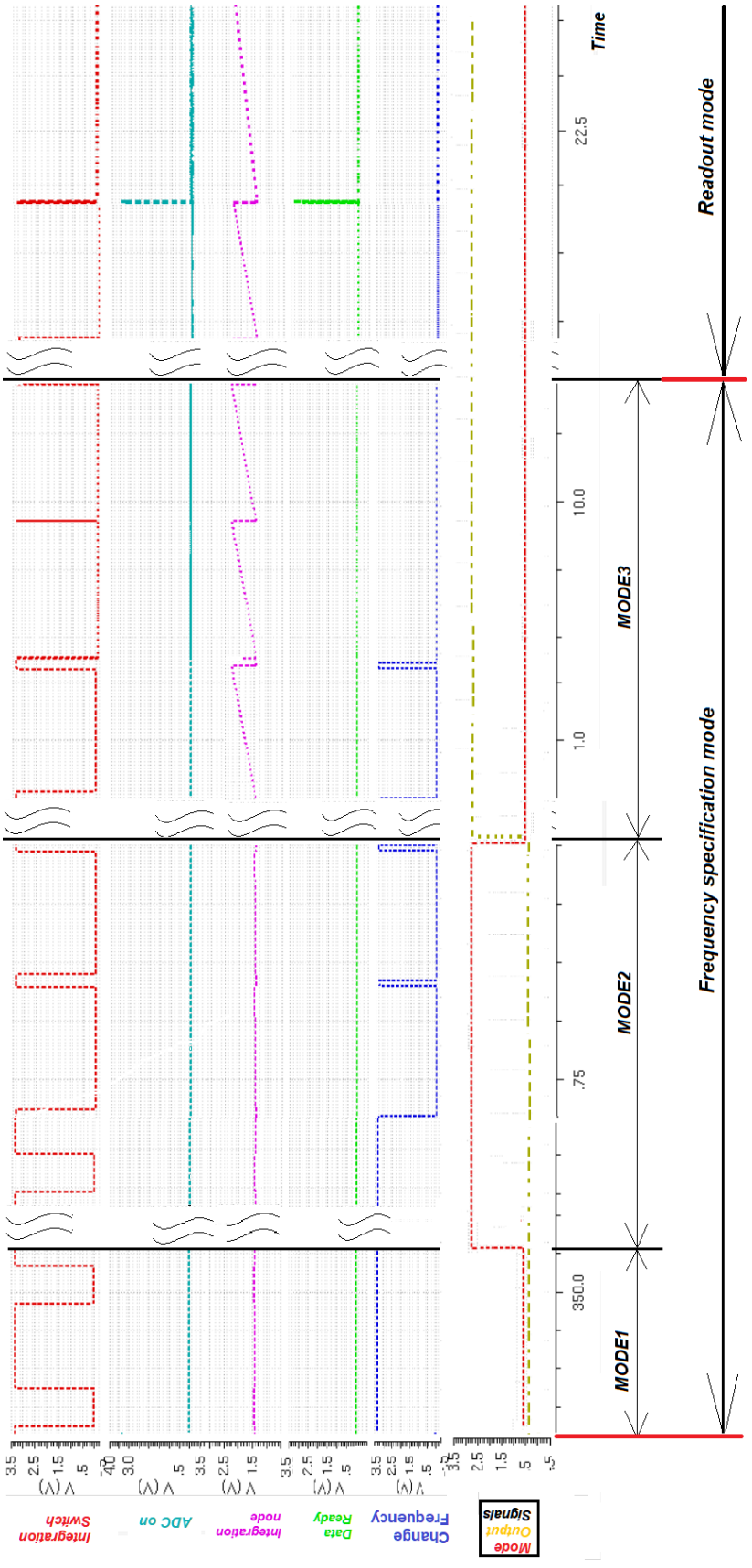

Figure 6.25: Sequence diagram

Chapter 7

Conclusion

7.1 Conclusion

THis thesis introduces a completely new topology. The circuit that has been developed can increase the capabilities of the biosensors significantly. As it has been pointed out, personalized medicine contributes to the improvement of the quality and the reduction of the cost of the treatment as it provides faster test results and reduces the cost of the clinical analysis. Biosensors are an important part of the personalized medicine concept. So, an improvement on the functionality of the biosensors is a serious step forward.

The AMS circuit designed at this thesis can autonomously measure a wide range of read out currents which express the concertation of certain metabolites. It is the first time that such wide range of currents can be measured automatically. The results and specifications of the design prove that would be extremely beneficial to expand the concept of the autonomous biosensor measurements. The area and the power that need to be sacrificed can be counterbalanced by the reduction of the complexity.

7.2 Achievements

- The derivation of an readout circuit capable to measure a wide range of the current generated by the biosensor autonomously.
- The switch timing organization to limit charge injection issues, to ensure correct measurement and to avoid instability at the whole range of currents.
- The design of digital circuit as a feedback of the readout circuit using a hardware description language and then implementation of that circuit using standard cells.
- The management of interaction between the readout part and the feedback digital part.

7.3 Future work

Future work would include expansion of the capabilities of the designed topology. A very important achievement of this work is the derivation of a technique that fixes the offset created at the integration of big currents. Therefore, the measuring range could be expanded at both higher and lower measurements easily. Measuring different ranges of currents using the same principles introduce at this work could be useful at the monitoring of other metabolites than glucose. So, chips based on the same principle could be expanded to other biosensors.

A significant improvement that could take place at future work further improvements at the layout. Although postlayout simulations were not very disappointing, further improvement can be achieved. Focusing more on the specific nets and objects that add parasitic capacitances and change the behaviour of the circuit could take place. That would lead to more accuracy and linearity of the postlayout results that depict more realistic measurements.

Bibliography

[1] S. S. Ghoreishizadeh, "Integrated Electronics to Control and Readout Electrochemical Biosensors for Implantable Applications," Ph.D. dissertation, COLE POLYTECHNIQUE FDRALE DE LAUSANNE, the Netherlands, 2015.

[2] H. Mazhab-Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Trans. on Circuits and Systems*, vol. 60-I, pp. 1149–1157, 2013.

[3] M. Ahmadi and G. Jullie, "Current-mirror-based potentiostats for three-electrode amperometricel ectrochemical sensors," in *Circuits and Systems I:Regular Papers, IEEE Transactionson*, July 2009, p. 13391348.

[4] M. M. Ahmadi and G. A. Jullien, "Current-mirror-based potentiostats for three-electrode amperometric electrochemical sensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 56, no. 7, pp. 1339–1348, July 2009.

[5] S. Hwang and S. Sonkusale, "Cmos vlsi potentiostat for portable environmental sensing applications," *IEEE Sensors Journal*, vol. 10, no. 4, pp. 820–821, April 2010.

[6] M. Stanacevic, K. Murari, A. Rege, G. Cauwenberghs, and N. V. Thakor, "Vlsi potentiostat array with oversampling gain modulation for wide-range neurotransmitter sensing," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 1, pp. 63–72, March 2007.

[7] G. D. Micheli, S. S. Ghoreishizadeh, C. Boero, F. Valgimigli, and S. Carrara, "An integrated platform for advanced diagnostics," in *2011 Design, Automation Test in Europe*, March 2011, pp. 1–6.

[8] C.Hiemke, "Zur Elektrodynamik bewegter Körper," *European Journal of Clinical Pharmacology*, vol. 64, no. 2, p. 159166, 2008.

[9] P. Orazio, "Biosensors in clinical chemistry-2011update," *Clinica ChimicaActa*, vol. 412, no. 19, p. 17491761, 2011s.

[10] F. Valgimigli, "Evaluating the clinical accuracy of glucomenday: A novel microdialysis-basedcontinuousglucosemonitor,Journal of Diabetes ScienceTechnology," vol. 4, p. 11821192, 2010.

[11] C. M. Nguyen, J. Mays, H. Cao, H. Allard, S. Rao, and J. C. Chiao, "A wearable system for highly selective l-glutamate neurotransmitter sensing," Jan 2015, pp. 1–3.

[12] S. Lafi, A. Khalfallah, and M. S. Bouhlel, "A cholesterol lesion detection approach based on svd decomposition," Dec 2016, pp. 503–508.

[13] L. M. Borland and A. C. Michael, "An introduction to electrochemical methods in neuroscience," Available at https://www.ncbi.nlm.nih.gov/books/NBK1845/.

[14] N. A. Nordin, A. J. Jamil, A. S. C. M. Som, W. F. H. Abdullah, Z. M. Zain, U. M. A. Hamid, and S. Rani, "Potentiostat readout circuit design for a 3-electrode electrochemical biosensing measurement system," in *2016 7th IEEE Control and System Graduate Research Colloquium (ICSGRC)*, Aug 2016, pp. 159–163.

[15] H. J.Harris, "A time-based vlsi potentiostat for ion current measurements," in *Sensors Journal, IEEE*, vol. 4, no. 2, April 2006, p. 239247.

[16] S. S.Sonkusale, "Cmos vlsi potentiostat for portable environmental sensing applications," in *Sensors Journal, IEEE*, vol. 10, no. 4, April 2010, p. 820821.

[17] A.ZekiandH.Kuntman, "Accurate and high output impedance current mirror suitable for cmos current output stages," in *Electronics Letters*, vol. 33, no. 12, Jun 1997, p. 10421043.

[18] L. Li, X. Liu, W. A. Qureshi, and A. J. Mason, "Cmos amperometric instrumentation and packaging for biosensor array applications," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 5, no. 5, pp. 439–448, Oct 2011.

[19] H. M. Jafari and R. Genov, "Chopper-stabilized bidirectional current acquisition circuits for electrochemical amperometric biosensors," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1149–1157, May 2013.

[20] C. Yang, Y. Huang, B. L. Hassler, R. M. Worden, and A. J. Mason, "Amperometric electrochemical microsystem for a miniaturized protein biosensor array," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 3, no. 3, pp. 160–168, June 2009.

[21] P. M. Levine, P. Gong, R. Levicky, and K. L. Shepard, "Active cmos sensor array for electrochemical biomolecular detection," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 8, pp. 1859–1871, Aug 2008.

[22] Razavi., *Design of Analog CMOS Integrated Circuits.* McGraw Hill, 2001, "pg. 425", "417","415", "422".

[23] S. Smith., *Microelectronic Circuits.* Oxford University Press, 2010, "pg. 876".

[24] E. Salman and E. G. Friedman, "Methodology for placing localized guard rings to reduce substrate noise in mixed-signal circuits," in *2008 Ph.D. Research in Microelectronics and Electronics*, June 2008, pp. 85–88.

[25] D. Long, X. Hong, and S. Dong, "Optimal two-dimension common centroid layout generation for mos transistors unit-circuit," in *2005 IEEE International Symposium on Circuits and Systems*, May 2005, pp. 2999–3002 Vol. 3.

Appendix A

VHDL code of the Digital block

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;


-- this is the entity
ENTITY state_machine IS
   PORT(
      clk       : IN    STD_LOGIC;
      desicion     : IN    STD_LOGIC;
      reset     : IN    STD_LOGIC;
      frequency1    : OUT   STD_LOGIC;
      frequency2    : OUT   STD_LOGIC;
      frequency3    : OUT   STD_LOGIC;
      START : OUT  STD_LOGIC
      );
END state_machine;
ARCHITECTURE a OF state_machine IS

   signal count_reset:integer range 0 to 10:=0;
   signal count_change:integer range 0 to 10:=0;
   signal Make_change :STD_LOGIC;
   TYPE STATE_TYPE IS (s0, s1, s2, s3);
   SIGNAL state    : STATE_TYPE;
BEGIN
   PROCESS (clk, reset)
    variable temp_f:integer range 0 to 1000000:=0;
    variable temp_BIG:integer range 0 to 1000000:=0;
```

```
  variable temp_N:integer range 0 to 100:=0;
  variable var_one:integer range 0 to 16:=0;
BEGIN
   IF reset = '1' THEN
      state <= s0;
      START<='0';
      temp_BIG:=0;
      temp_N:=0;
      count_reset<=0;
      count_change<=0;
      Make_change<='0';
      var_one:=0;
      temp_f:=0;

   ELSIF (clk'EVENT AND clk = '1') THEN


      CASE state IS
         WHEN s0=>

        if count_reset = 10 then
           if count_change > 7 then
             state <= s1;
       count_reset<=0;
               count_change<=0;
       temp_f:=0;
       var_one:=0;
  else
     if (0 <= var_one and var_one <= 10) then
     if (0<temp_f and temp_f<12) then
               START<='1';
     else
       START<='0';
     end if;
     if (temp_f = 0) then
       var_one:=var_one+1;
     end if;
     else
     state <= s0;
             count_reset<=0;
                   count_change<=0;
     START <='0';
     var_one:=0;
     end if;
  end if;
       end if;
```

```
      temp_f:=temp_f+1;

       if(temp_f<=11)then
          frequency1<='1';
       else
         frequency1<='0';
       end if;

      if(temp_f<=9)then
        frequency2<='0';
      else
        frequency2<='1';
      end if;

      if(temp_f<=1)then
        frequency3<='0';
       elsif (1<temp_f and temp_f<6) then
        frequency3<='1';
if desicion = '1' then
              Make_change<='1';
elsif desicion = '0' then
  Make_change<='0';
      end if;

      elsif (temp_f>6) then
         frequency3<='0';
      end if;


    if(temp_f=12)then
          temp_f:=0;
if(var_one=0)then
           count_reset<=count_reset + 1;
end if;
             if Make_change = '1' then
  if(var_one=0)then
                  count_change<=count_change + 1;
  end if;
            end if;
     end if;

        WHEN s1=>

        if count_reset = 10 then
           if count_change > 7 then
```

```
                    state <= s2;
        count_reset<=0;
                 count_change<=0;
        temp_f:=0;
        var_one:=0;
    else
        if (0 <= var_one and var_one <= 10) then
        if (0<temp_f and temp_f<12) then
                 START<='1';
        else
          START<='0';
        end if;
        if (temp_f = 0) then
          var_one:=var_one+1;
        end if;
        else
        state <= s0;
                count_reset<=0;
                      count_change<=0;
        START <='0';
        var_one:=0;
        end if;
    end if;
          end if;

         temp_f:=temp_f+1;

          if(temp_f<=11)then
             frequency1<='1';
          else
            frequency1<='0';
          end if;

         if(temp_f<=9)then
           frequency2<='0';
         else
           frequency2<='1';
         end if;

         if(temp_f<=1)then
           frequency3<='0';
          elsif (1<temp_f and temp_f<6) then
           frequency3<='1';
    if desicion = '1' then
                 Make_change<='1';
    elsif desicion = '0' then
```

```
    Make_change<='0';
        end if;
       elsif (temp_f>6) then
          frequency3<='0';
       end if;


      if(temp_f=44)then
            temp_f:=0;
  if(var_one=0)then
              count_reset<=count_reset + 1;
  end if;
               if Make_change = '1' then
                 if(var_one=0)then
                    count_change<=count_change + 1;
    end if;
               end if;
       end if;


          WHEN s2=>
          if count_reset = 10 then
             if count_change > 7 then
                 state <= s3;
        count_reset<=0;
                 count_change<=0;
        temp_f:=0;
        var_one:=0;
  else
       if (0 <= var_one and var_one <= 10) then
       if (0<temp_f and temp_f<12) then
                 START<='1';
       else
         START<='0';
       end if;
       if (temp_f = 0) then
         var_one:=var_one+1;
       end if;
       else
       state <= s0;
              count_reset<=0;
                    count_change<=0;
       START <='0';
       var_one:=0;
       end if;
  end if;
```

```
        end if;

       temp_f:=temp_f+1;

        if(temp_f<=11)then
           frequency1<='1';
        else
          frequency1<='0';
        end if;

       if(temp_f<=9)then
         frequency2<='0';
       else
         frequency2<='1';
       end if;

       if(temp_f<=1)then
         frequency3<='0';
        elsif (1<temp_f and temp_f<6) then
         frequency3<='1';
if desicion = '1' then
              Make_change<='1';
elsif desicion = '0' then
  Make_change<='0';
      end if;
      elsif (temp_f>6) then
         frequency3<='0';
      end if;


     if(temp_f=1227)then
          temp_f:=0;
if(var_one=0)then
            count_reset<=count_reset + 1;
end if;
             if Make_change = '1' then
                   if(var_one=0)then
                   count_change<=count_change + 1;
  end if;
             end if;
      end if;

         WHEN s3=>
        if count_reset = 10 then
           if count_change > 7 then
               state <= s0;
```

```
        count_reset<=0;
                count_change<=0;
        temp_f:=0;
        var_one:=0;

    else
        if (0 <= var_one and var_one <= 10) then
        if (0<temp_f and temp_f<12) then
                START<='1';
        else
          START<='0';
        end if;
        if (temp_f = 0) then
          var_one:=var_one+1;
        end if;
        else
        state <= s0;
                count_reset<=0;
                      count_change<=0;
        START <='0';
        var_one:=0;
        end if;
    end if;
          end if;

         temp_f:=temp_f+1;

          if(temp_f<=11)then
             frequency1<='1';
          else
            frequency1<='0';
          end if;

          if(temp_f<=9)then
            frequency2<='0';
          else
            frequency2<='1';
          end if;

          if(temp_f<=1)then
            frequency3<='0';
           elsif (1<temp_f and temp_f<6) then
    if desicion = '1' then
                Make_change<='1';
    elsif desicion = '0' then
      Make_change<='0';
```

```
          end if;
            frequency3<='1';
         elsif (temp_f>6) then
            frequency3<='0';
         end if;


        if(temp_f=40949)then
              temp_f:=0;
    if(var_one=0)then
              count_reset<=count_reset + 1;
    end if;
                if Make_change = '1' then
                      if(var_one=0)then
                     count_change<=count_change + 1;
      end if;
                end if;
         end if;

         END CASE;

      END IF;
   END PROCESS;


END a;
```