Wired Full-Duplex Communication and Power Delivery for Medical Implantable Systems.

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Abstract

Emerging applications for implantable devices require multi-node systems with intrabody transmission of power and data through wireline interfaces. Forming part of the CANDO project, this work provides the design and implementation of a PCB-based, master chest device. It focuses on achieving an efficient and AC-coupled system; providing an interface for power delivery and full-duplex data communication. Such an interface is used by a single master and multiple slave devices; utilising a parallel-connected 4-wire implantable cable. A novel adaptive power delivery method that makes use of closed loop dynamic regulation is being proposed. Regulation is attained within the master unit by closed loop monitoring of the current consumption flowing through the wired link. Simultaneous power transfer and full-duplex data communication are achieved by superimposing the power carrier and downlink data over two wires, and the uplink data over a second pair of wires. Measured results using a fully isolated (AC coupled) 4-wire lead, demonstrate that this implementation can transmit up to 120 mW of power at 6 V (at the slave device, after eliminating any losses). The master device has a maximum system efficiency of 86 %, with a dominant dynamic power loss, and a maximum power transmission efficiency of 50 %. A 6 V constant supply at the slave device is recovered 1.5 ms after a step of 22 mA. Downlink and uplink communication are achieved at a bit rate of 100 kbps and 1.6 Mbps respectively. The achieved bit error rate of the uplink is less than 1 %.

Acknowledgments

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I would like to extend my gratitude to Nelson Gomes for our constant discussions, mostly centering on our respective projects. A special thank you goes to Daryl and Wei for the interesting conversations we had in the Bessemer building whilst we were all working on our respective projects.

I also want to thank Karim Elmantawi and Tahmid Ahmed for the breaks we had; playing pool when we felt the need for some time off from the MSc course. Additionally, I would like to thank my colleagues on the 9th floor in the EEE building, for the jokes and the interesting conversations we had throughout the year.

Finally, I would like to express my heartfelt gratitude to my family; my parents, for their support, patience, encouragement and help throughout the thesis; and my sisters for always finding a way to cheer me up, even when I felt stressed and met with problems that needed to be solved during the course of this project.

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List of Abbreviations

μLED	micro Light Emitting Diode
4WIC	4-Wire interface Integrated Circuit
AC	Alternating Current
ADC	Analogue to Digital Converter
ASIC	Application Specific Integrated Circuit
BER	Bit Error Rate
BJT	Bipolar Junction Transistor
CAN	Controller Area Network
CANDO	Controlling Abnormal Network Dynamics using Optogenetics
CI	Central Implant
DC	Direct Current
digPOT	Digital Potentiometer
EMI	Electromagnetic Interference
FES	Functional Electrical Stimulation
FPGA	Field Programmable Gate Array
FSK	Frequency Shift Keying

FSM	Finite State Machine
GUI	Graphical User Interface
I/O	Input/Output
IC	Integrated Circuit
IMD	Implantable Medical Device
LED	Light Emitting Diode
LFP	Local Field Potential
LPF	Low Pass Filter
LSB	Least Significant Bit
LSK	Load Shift Keying
MA	Moving Average
MICS	Medical Implants Communication Service
MLT	Multi-Level Transmit
MOSFET	Metal-Oxide Semiconductor Field Effect Transistor
MSB	Most Significant Bit
NC	Normally Closed
NNP	Networked Neuroprosthesis
NO	Normally Open
NRZ	NonReturn-to-Zero
PC	personal computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PCU	PCB based Chest Unit

PCU_v1	PCB based Chest Unit version 1
PCU_v2	PCB based Chest Unit version 2
PI	Peripheral Implant
PLL	Phase Locked Loop
PM	Peripheral Module
PTE	Power Transmission Efficiency
PWM	Pulse Width Modulation
RF	Radio Frequency
ROM	Read Only Memory
SPDT	Single-Pole, Double-Throw
SPI	Serial Peripheral Interface
SPST	Single-Pole, Single-Throw
UART	Universal Asynchronous Receiver/Transmitter
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit

Chapter 1

Introduction

1.1 Motivation

SINCE the first pacemaker, research has come a long way in the field of implantable devices and systems. With increasing system complexity, new implantable systems are emerging, such as the implantable drug delivery system and visual prosthesis. The latest type of an implantable system consists of several devices, one of which is the master device. This has resulted in a demand for an interface/protocol that can deliver power and obtain full-duplex data communication between the master and the identical slave modules.

Such interface and its implementation need to be: reliable, to guarantee uninterrupted power delivery with a constant supply; efficient, to minimise heat losses and prolong battery life; and have no DC leakage to ensure that no static current flows through the body in case of failure. There has been significant effort in the academic community on developing various wireless interfaces to satisfy these requirements. Even so, the majority of such interfaces are wired, using an implantable cable with optimal mechanical properties.

Hence the objective of this thesis is to present a particular implementation of a master device, and the electronics required to interface with multiple slave devices. A novel power delivery architecture is also presented and adopted in this work; thereby designing a closed-loop system which adapts the voltage at the master device, depending on the current flowing through the slave devices. Whilst the master to slave data communication

is encoded in the power signal, using two wires, another two wires are used for the slave to master data communication. The whole design is implemented on two PCBs, one being a custom designed board, whilst the other is an FPGA board, which is used to interface with the electronic components on the other board. The design can be controlled by a developed GUI.

1.2 Thesis Outline

This thesis is structured as follows:

Chapter 2, *Background*, provides an insight into the types of implantable systems found in the literature, and the several interfaces that are used in multi-module implantable systems.

Following this, **Chapter 3**, entitled *Project Contribution within CANDO*, provides the context in which this work was carried out and the objectives set for this project.

In **Chapter 4**, *Hardware Design*, the system architecture is presented and described. The various subsystems of the system architecture are tackled separately, facilitating system implementation. This Chapter further delves into the identification of the components required for each subsystem, as well as, their selection process. The different stages in the hardware design process are also described in detail.

On the other hand, **Chapter 5**, *Software Design*, describes the design of the necessary firmware for the FPGA and the GUI (used to control the final system).

Chapter 6, *Testing, Results and Discussion*, details the testing conducted throughout the whole process; from the systems initial manufacture till its completion; when system performance was tested. The system characteristics obtained through the performance testing, are then discussed.

Finally, in the *Concluding* Chapter, the results obtained are summarised, and future work in improving the system and possible applications are discussed.

Furthermore the publication arising from this work is attached in **Appendix A**.

1.3 Contributions

The main contributions towards the Controlling Abnormal Network Dynamics using Optogenetics (CANDO) project resulting from this work are outlined below:

1. An adaptive and closed loop power delivery architecture that can deliver up to 120 mW to the slave device.
2. A switch based driver architecture that can operate up to 11 V for both power and data delivery to the slave device at a rate of 100 kHz.
3. A feedback system, free of a current sensing resistor, with a maximum sampling rate of 100 kSps and a settling time of 100 µs.
4. A configurable receiver architecture that can decode phase encoded data received from the slave device at bit rates of 800 kbps and 1.6 Mbps.

Chapter 2

Background

THE field of micro and nano technology has come a long way since Feynman's lecture in 1959, entitled *There's plenty of room at the bottom*. It is thanks to these technologies that it is possible to design and execute more complex implantable systems, with this project being a testament to that.

Thus, this Chapter presents information on implantable systems and their challenges to enable the reader to better understand such systems. Section 2.1 introduces the field of implantable systems and focuses on the two most common types of systems, namely single-device and multi-module implantable systems. The following section, Section 2.2, elaborates on wired intrabody power and data communication, targeting specifically the interface used between multi-module implants.

2.1 Implantable Systems

Implantable Medical Devices (IMDs) such as cochlear implants, pacemakers and deep brain stimulators have already demonstrated a significant impact on the quality of life of millions of users. These devices interface with the human body by monitoring and/or manipulating activity, and are able to restore function by bypassing dysfunctional organs/pathways. Although the field of IMDs is not new (in fact the first implantable pacemaker dates back to 1959), with the advent of microtechnology and the capability that this brings, the ambition and reach of such devices are now targeting significantly more advanced

diseases/treatments. Some examples include: neural prostheses for depression, eating disorders and epilepsy [1]. The design of such systems entails deciding whether to use a single-device system or a multi-module system.

2.1.1 Single-device Implantable Systems

A single-device system comprises of a centralised module which performs most of the necessary functions for its intended application. This device is able to manage its power, obtain data from its sensors, and actuate/stimulate its peripherals. The processing of the data obtained from its sensors can be performed externally (on another device that is external to the body) or internally, depending on the system's design and complexity. Additionally, battery charging and device programming is usually done by using a Radio Frequency (RF) link between the implanted and external devices, as shown in Figure 2.1. Examples of single-module implantable systems are pacemakers, cochlear implants and implantable neuroprosthesis for limb function restoration, as illustrated in Figures 2.2a and 2.2b.

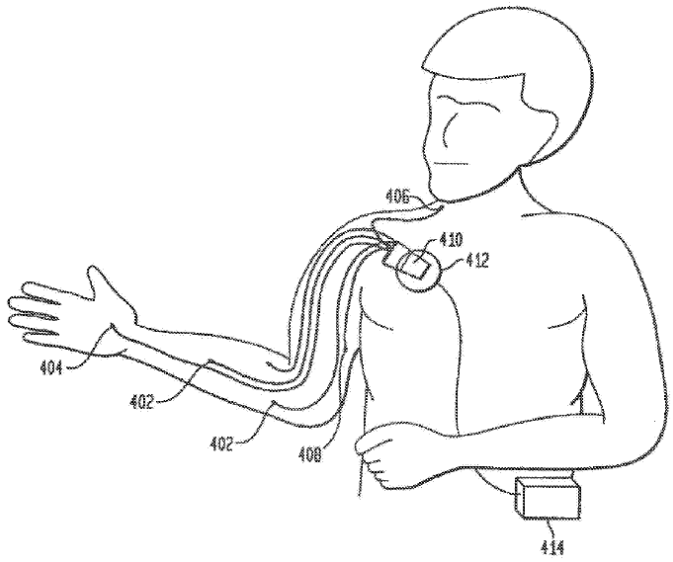
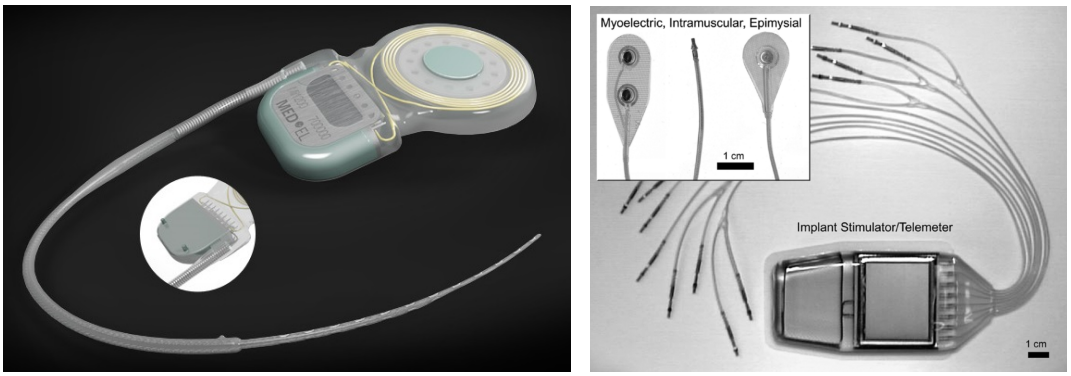


Figure 2.1: An example of a single-module implantable system - 402-408 are recording/stimulating electrodes | 410 is the main implantable device | 412 is the inductive link for external communication | 414 is the external control unit [2].

A single-module system however, can only address one specific function/disability, and it cannot be extended to work beyond the application for which it was designed.



(a) A cochlear implant [3]. **(b) A device used for the restoration of limb function [4].**

Figure 2.2: Examples of single-device implantable systems.

Designing it for multiple disabilities will lead not only to a considerable increase in system complexity and cost, but also to a reduction in reliability. Thus, it is difficult to address multiple disabilities with only one centralised device [5] [6]. An emerging approach to mitigating such challenges is to employ multi-module or multi-node implants.

2.1.2 Multi-module Implantable Systems

In a multi-module structure, the system is effectively partitioned into physically-separated units, with the different functions located at different sites, as illustrated in Figure 2.3. The most common configuration is to have one relatively large Central Implant (CI), typically implanted in the upper chest that houses the battery, processing and communication functions. Smaller Peripheral Implants (PIs) can then be located close to the target interface sites.

One good example is the Networked Neuroprosthesis (NNP) system developed at Case Western Reserve University [5] [7] as exhibited in Figure 2.4. This system is based on four basic components, namely the *Power module* which delivers power to the other modules and provides a way to program the system; *Actuator modules*; *Sensor modules*; and a *Network Cable* providing a connection for these modules. As this is however, targeted to Functional Electrical Stimulation (FES) applications, the required number of stimulation and/or recording channels (and bandwidth) is limited.

A similar example is the patented design by Sun Microsystems [6]. It consists of a

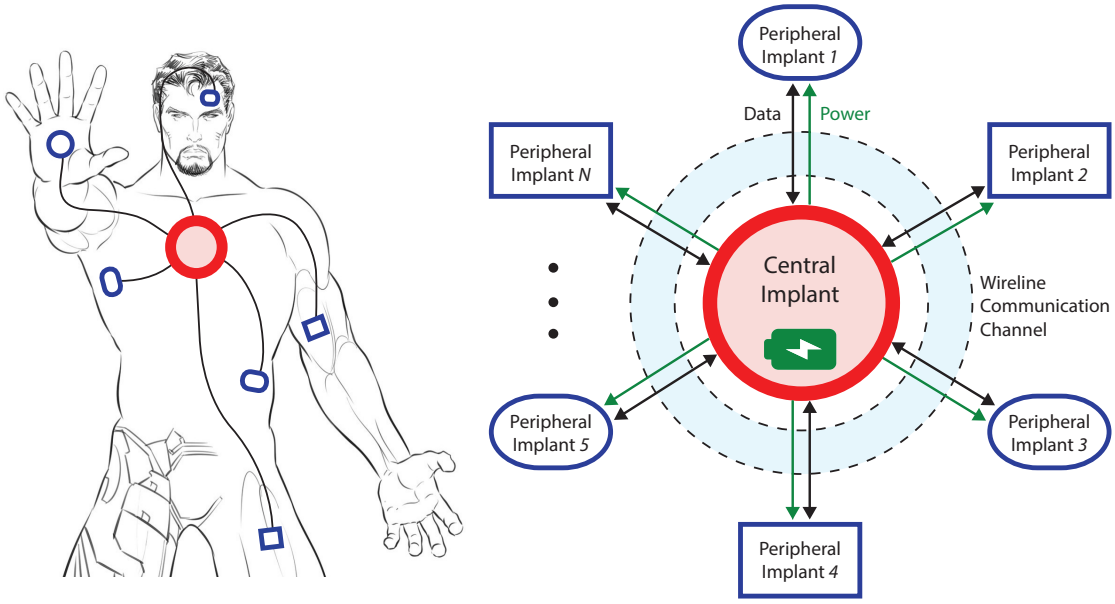


Figure 2.3: The concept of wired intrabody multi-module implants.

network of two or more subcutaneously/transdermally implanted devices. These devices can perform either monitoring (such as, measuring a physiological parameter) or intervention (for example, drug delivery or stimulus) functions. Additionally, the network can either be hard-wired (electrically or using an optically conductive material) or a wireless interface.

2.1.3 Comparison of Single and Multi-module Implantable Systems

Table 2.1 notes the differences between single and multi-module systems.

Table 2.1: Comparison between single and multi-module implantable systems.

	Upgrades	Addressing multiple disabilities	Sensing/Stimulating different locations in the body
Single module	Need to redesign the whole system or device.	Not a viable solution to have an independent single-module system for each disability.	Requires wires from each sensor/actuator to the main module.
Multi module	Need to redesign only one module.	Can have one system which addresses all disabilities using multiple application specific modules.	All modules can share the same cable. Additionally, modules can include a processing element to reduce data rate to be sent to the CI.

The work presented in this thesis forms part of a bigger project, namely, the

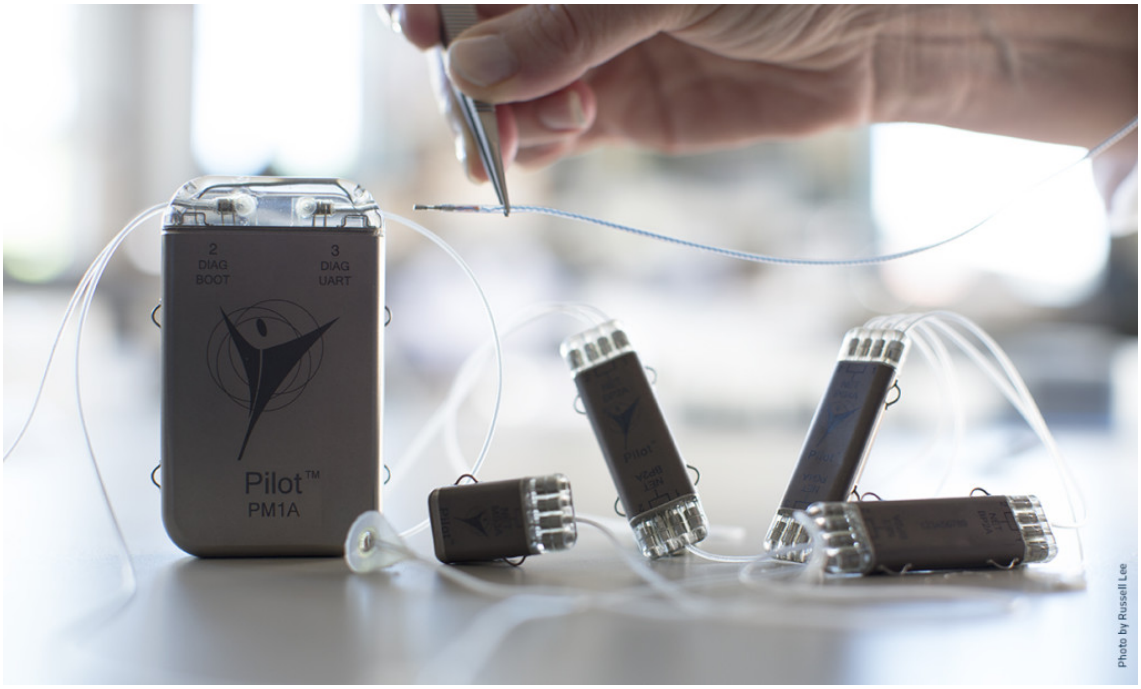


Figure 2.4: The NNP system by Case Western Reserve University [8].

CANDO project (www.cando.ac.uk). CANDO aims at developing an implantable system to provide a closed-loop therapy for focal epilepsy. The CANDO system consists of one CI unit for control and power delivery and multiple PIs for bidirectional neural interfacing [9]; thereby constituting a multi-module system. The different implants are connected via a shared implantable lead.

2.2 Intrabody Power delivery and Data Communication

The need to reliably transmit power from a single CI to multiple PIs poses certain challenges. It is imperative that any configuration adopted is safe, reliable and efficient. For these reasons, the majority of such links are wire-based despite the fact that there has been significant effort in academia on developing various wireless modalities [10], such as the Medical Implants Communication Service (MICS) specification. Even so, wire-based transmission poses certain challenges as described below:

- The number of wires must be kept to a minimum to reduce cost and minimise the number of wires that may fail.
- DC voltages must be avoided to reduce the risk of corrosion and tissue damage in

case of device/cable failure [11].

- Power transfer has to be as efficient as possible whilst using a safe and implantable cable, as any heat loss will contribute to a temperature rise in the tissue, which may result in damaged tissue [12].
- The interface (or protocol used) must guarantee uninterrupted power delivery (and data communication) with a constant supply at the PIs irrespective of battery level, a load that changes with configuration, and a dynamic current profile; thus ensuring reliable system operation.

2.2.1 Power Delivery and CI to PI Communication

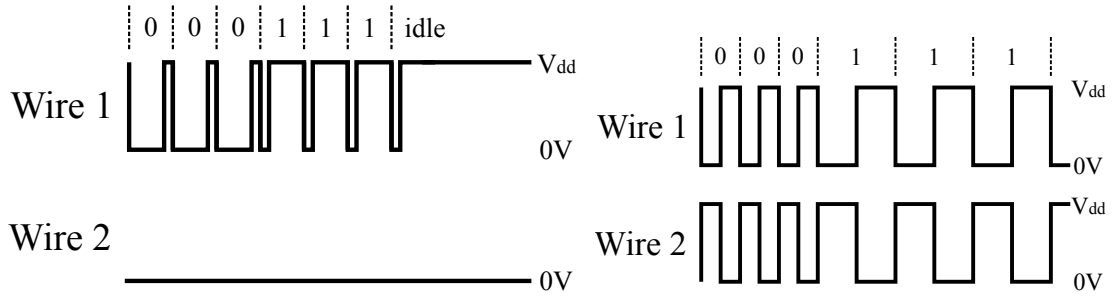
As is always the case with an electronic system, each subsystem requires power to provide the functionality it was designed for. Thus, this section describes several of the interfaces found in the literature that deliver power and also send data to one or more PIs.

2.2.1.1 Pulse Width Modulation

Pulse Width Modulation (PWM) makes use of the pulse width to store information. In the case of digital logic, since there are only two states (0 or 1), these can be represented by a short and a long pulse respectively. In fact, [13] send data to their implantable electrode-driving Application Specific Integrated Circuit (ASIC) by using PWM. During idle operation, this signal is a constant DC voltage. In conjunction with a ground wire, the PWM signal powers also the ASIC. In this case, to distinguish between a logic 0 and a logic 1, the duty cycle of the pulse is varied, as illustrated in Figure 2.5a. However in [14], the duty cycle is kept constant, and the frequency of the pulse is adjusted to get a different pulse width (similar to Frequency Shift Keying (FSK)), as depicted in Figure 2.5b.

2.2.1.2 Manchester Encoding

Another way to communicate and deliver power to the PI unit, is by using phase encoding on the bit-stream, as found in [15] [16]. The phase encoded data stream, in conjunction with an inverted version driven on another wire power the PI. This encoding results in



(a) PWM data as found in [13]. (b) PWM data as used in [14].

Figure 2.5: PWM timing diagram as used in the literature.

a continuous square wave (even during no data transmission) with a cycle equal to the inverse of the bit rate. Like PWM, this interface requires synchronisation, to signal that a data packet will be sent. Manchester encoding can also be used for PI to CI communication as implemented in [15].

2.2.2 PI to CI communication

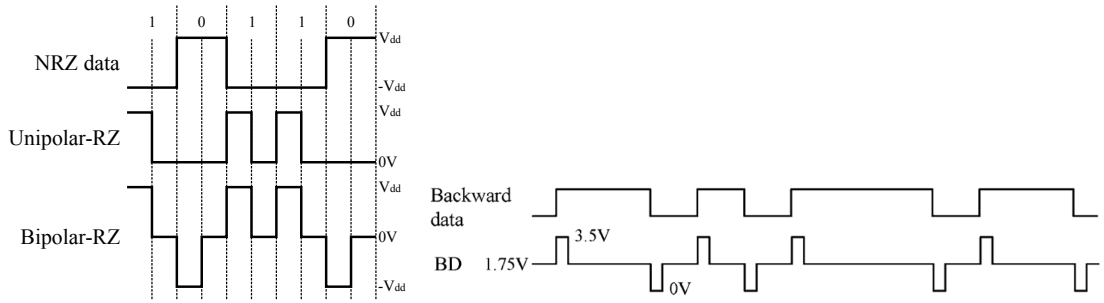
Apart from CI to PI communication, the opposite may also be required, especially for sensor modules that need to send data back to the main module. Thus, this section outlines the interfaces found in the literature for this direction of communication.

2.2.2.1 Pulse Code Modulation

Pulse Code Modulation (PCM) is a modulation technique that is used to represent a sampled analogue signal as a series of pulses. There are different ways however, to apply these pulses to the digital bit stream, as shown in Figure 2.6a. [16] applies PCM as shown in Figure 2.6b. This implementation uses high frequency pulses (as their pulse width is smaller than that of the data) to mark a change in the data. A rising edge followed by a falling edge signifies a 1, whilst the opposite implies a 0.

2.2.2.2 Load Shift Keying

In Load Shift Keying (LSK), the current flowing through the PI is modulated according to the bit stream that needs to be sent to the CI. As implemented in [14], in the case of sending a 1, the quiescent current is decreased by opening the implemented switches,



(a) Ways to apply PCM to a bit stream. NRZ – Nonreturn-to-zero | RZ – Return-to-zero.

(b) PCM as implemented in [16].

Figure 2.6: Different ways to modulate data using PCM.

whilst should a 0 be required, no operation is performed. This results in short pulses at the CI when a 1 is sent, which are then recovered by a comparator on the central implant. Similar to previous modulation techniques, a synchronisation packet is required before sending data.

2.2.2.3 Controller Area Network

Though Controller Area Network (CAN) was originally intended for automotive applications, it has also been used in IMDs [7] [17]. As defined by ISO 11898, CAN uses differential data transmission on two wires. The standard defines a bus that must be terminated by using a resistor of 120 Ω at each end of the bus. The protocol uses NonReturn-to-Zero (NRZ) with bit-stuffing to ensure that other modules are synchronised. Additionally, logic 0 is dominant in the bus, so that data transmission is prioritised. This means that when a module transmits a 1, but the bus is at a logic low, the module stops transmitting and becomes a receiver instead (arbitration).

2.2.3 Comparison of Various Protocols/Interfaces

Table 2.2 notes the differences (in the context of IMDs) between the interfaces discussed in this section. The interface chosen for the CANDO project [15] uses phase encoding for both CI to PI communication and vice-versa, since this constitutes the optimal solution. A phase encoded interface is charge balanced, efficient, can be capacitively coupled, and a clock can be synthesised from it on both CI and PI sides.

Table 2.2: Comparison of the interfaces used for intrabody communication.

	PWM as [13]	PWM as [14]	Phase encoding as [15] [16]	PCM as [16]	CAN
Power Delivery	Yes	Yes	Yes	No	No
Charge Balanced	No, because duty cycle $\neq 50\%$.	Yes	Yes	Yes, since a pulse is applied on the edges of the data.	No, because data is NRZ. This is reduced with bit stuffing.
Can it be capacitively coupled?	No	Yes	Yes	Yes	Yes, but would not comply with standard ISO 11898.
Can a clock signal be extracted?	Yes*	Yes*	Yes*	No, especially for many consecutive ones/zeros.	No, especially for many consecutive ones/zeros.
Efficient Drivers, and Low power	Yes	Yes	Yes	Yes	No, because of the termination resistor.
Bit time	Constant	Has 2 lengths	Constant	Constant	Constant

* If bit stream is continuous – transmission does not stop.

Chapter 3

Project Contribution within CANDO

AS mentioned in the previous chapter, CANDO aims at developing an implantable system to provide a closed-loop therapy for focal epilepsy. This is done by continuously monitoring Local Field Potentials (LFPs) in the brain, identifying abnormal activity, and modulating such activity by optically stimulating genetically modified cells. To target multiple cells, multiple devices (called optrodes) are required at different locations. Additionally, since these optrodes will be implanted in the brain, space will be limited; which is why a master device (implanted in the chest) is required as illustrated in Figure 3.1.

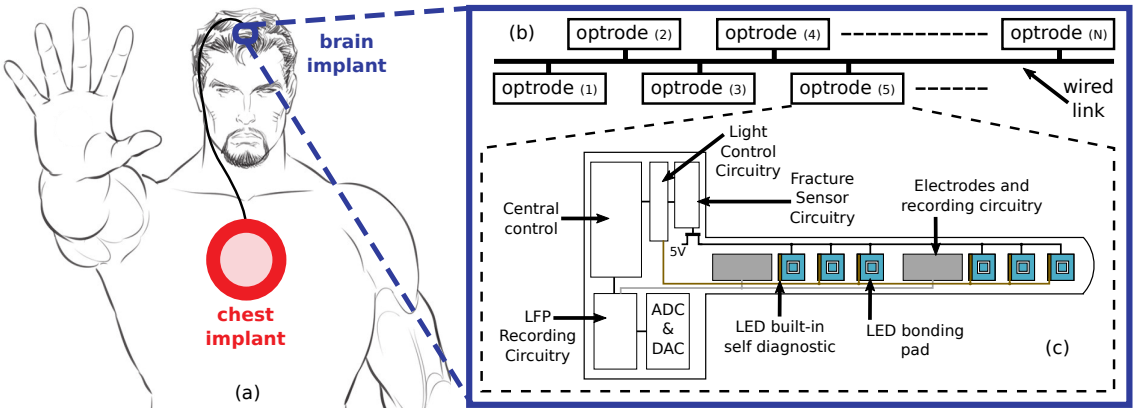


Figure 3.1: System architecture for CANDO; (a) general overview; (b) brain implant consisting of multiple optrodes (N can be 2–16); (c) an optrode, adapted from [18].

3.1 CANDO – System Overview

A holistic view of the final system as required by CANDO is shown in Figure 3.2.

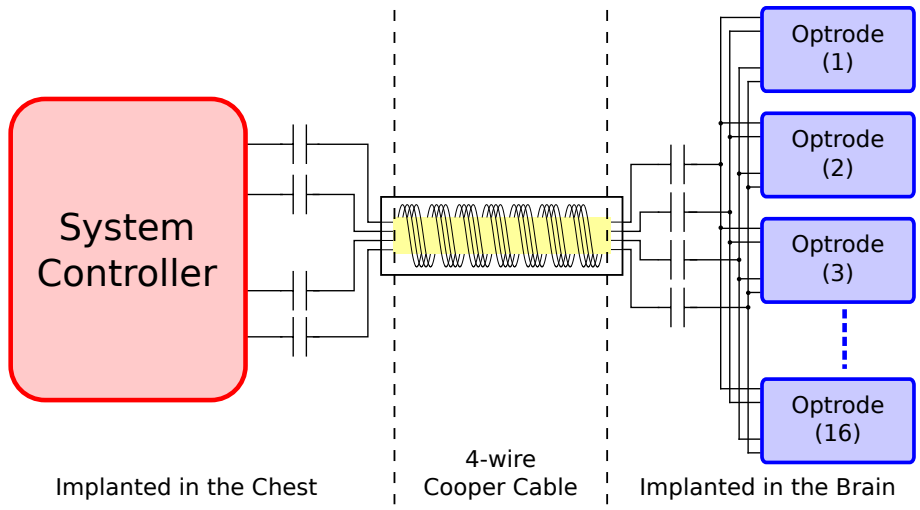


Figure 3.2: The CANDO implantable system.

This implantable system is divided into three main elements namely:

1. **Brain Implant (consisting of multiple optrodes)** – An optrode is responsible for acting upon the commands received from the chest implant (for example, transmitting LFP recordings to the chest implant, or stimulating a specific neuron by switching on a micro Light Emitting Diode (μLED)).
2. **Cooper Cable** – This cable is required as a communication medium between the chest and the brain implant for successful power delivery and full duplex data communication.
3. **Chest Module** – This module is responsible for powering all optrodes, processing the data received from LFP recordings and sending the required commands to the optrodes. It is also responsible for communicating with other devices external to the body, system monitoring, and battery charging.

The following highlights the electrical specifications of each element in the system. Most of this information is a summary of [15].

3.1.1 The Brain Implant

The optrodes require an internal supply of 5 V to operate. This is obtained through a rectifier which converts the received differential square wave generated by the chest implant to a DC voltage. The rectifier has an approximate voltage drop of 1.15 V (changes slightly at different loads). The quiescent current of one optrode when it is idle is 0.2 mA. During stimulation periods, this value increases to a maximum of 2.6 mA, of which 2.3 mA is used to switch on a μLED placed on the optrode (thus most of the load is resistive). If 16 optrodes (this is the maximum) are available in the brain implant, a maximum of 8 optrodes (1 μLED each) can be stimulating at the same time.

3.1.2 The Communication Medium

In the current set-up of the CANDO system, the communication medium used is a 77 cm, 4-wire Cooper cable as illustrated in Figure 3.3. Each wire in the cable has the following characteristics per unit length (cm): an inductance of 25 nH, a resistance of 2 Ω, a capacitance (between two adjacent wires) of 1.5 pF, and a capacitance (between two non-adjacent wires) of 1.2 pF [19].

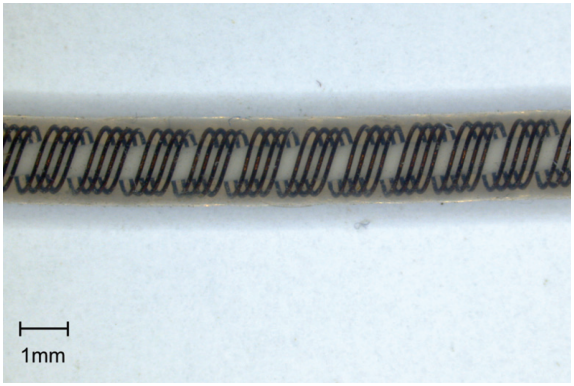


Figure 3.3: A 4-core Cooper cable.

3.1.3 The 4-Wire Interface

Chest to brain implant communication is achieved by using phase encoding on the bit stream. When no data needs to be sent, the bit is set to 0, hence sending a 50 % duty cycle square-wave voltage to power the Peripheral Modules (PMs). Brain to chest

communication uses also differential signalling and phase encoding. The connections are AC coupled on both sides (that is, both at the chest and the brain). The maximum bit rate for both chest to brain and brain to chest streams is 100 kbps and 1.6 Mbps respectively. The waveforms for both interfaces are depicted in Figure 3.4.

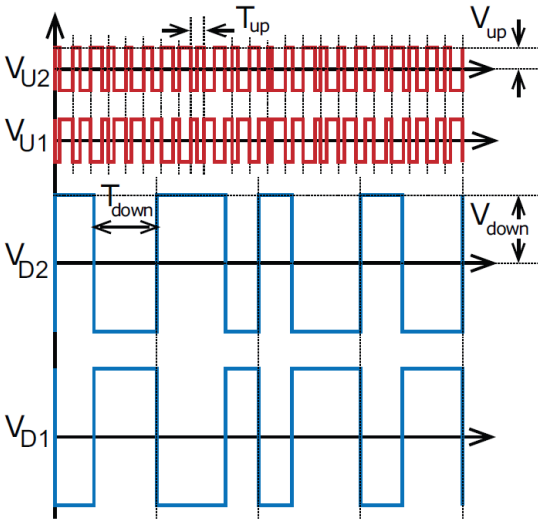


Figure 3.4: Ideal voltage waveforms on the 4-wires. Whilst subscripts D1 and D2 are for the chest to brain link, U1 and U2 are for the brain to chest link [15].

3.1.4 The Chest Device

This thesis focuses on the chest implant, specifically on the 4-wire interface which enables power delivery and full-duplex communication between the chest implant and the brain implant. Other functions required in the chest implant, such as the electronics for external communication, medical and electrical closed loop control algorithms, battery recharging and system supervision are not considered.

A high level view of the subsystems required in the chest device for the given application is illustrated in Figure 3.5. Furthermore, it should be noted that this author, from now onwards will start referring to the chest to brain connection as *downlink* and the brain to chest connection as *uplink*.

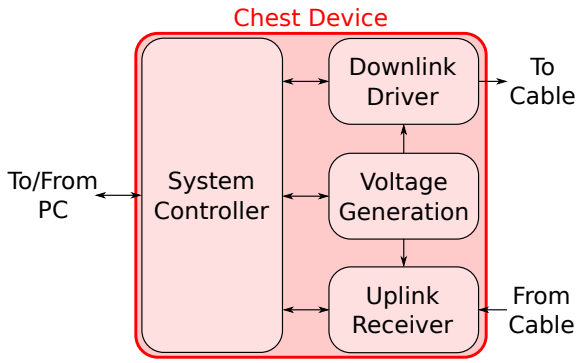


Figure 3.5: Top level view of the chest unit subsystem delivering power and communication to the brain implant.

3.2 Project Objectives

The system responsible for the 4-wire interface is designed by relying on modern Printed Circuit Board (PCB) technology. The software used for the design process, and generation of the gerber files for the PCB manufacturing is Altium Designer. The design specifications and objectives for this project are presented below:

- To implement a PCB based Chest Unit (PCU) which makes use of an efficient power delivery architecture to ensure minimal power losses in the system.
- To form a simple Graphical User Interface (GUI) which gives the ability to future users to control the system as necessary.
- To achieve or surpass the requirements set by the 4-wire interface (Table 3.1) and the components making up the system.

Table 3.1: System Requirements

Requirement	*Value*
Downlink	
Coupling	AC coupled
Supply level at brain implant	6 V
Maximum number of optrodes connected to system	16
Maximum number of optrodes stimulating at once	8
Downlink power supply efficiency	>80 %
Data packet width	24 bits
Synchronisation bits	10_2
Modulation	Phase encoding – square wave
Bit rate	100 kbps
Bit error rate	<1 %
Uplink	
Coupling	AC coupled
Packet width	24 bits
Modulation	Phase encoding – square wave
Synchronisation bits	10_2
Bit rates	800 kbps and 1.6 Mbps
Bit error rate	<1 %

Chapter 4

Hardware Design

THE previous Chapter outlined the context of this work and the various subsystems required. In so doing, it facilitates the process of identifying the required components for each block. Hence, this Chapter will first detail the decision process whereby the architecture (or specific component/s) are chosen to make part of a particular subsystem. This is then followed by an elaboration of the choice of the auxiliary components in ensuring proper functionality of this subsystem. Finally, once all the subsystems are planned, and the PCB of the whole system laid out, the design and implementation of the firmware used is also highlighted in the following chapter.

To ensure that the designed system meets the set objectives, hardware design was prioritised according to the subsystems; with the downlink driver having top priority, followed by the uplink receiver, and finally the power supply (voltage generation) subsystem. This was also done in order to reduce the number of iterations required during component selection, as the power supply depends on the choice of the components in the other subsystems.

Each subsystem is described in the following format:

1. The specifications of the subsystem are first explained and, if possible, derived.
2. Then, the component selection process is expounded upon by first comparing, and then selecting the different technologies (if applicable).
3. After a search for the appropriate components, the rationale behind the decision of

choosing a particular component is justified.

4. This is then followed by the schematic design, where the operation of the chosen component is explained, and other auxiliary components identified.
5. Last but not least, the particular techniques used in the PCB design are described.

Additionally, since two PCBs have been designed and assembled, the first one will be referred to as PCB based Chest Unit version 1 (PCU_v1) whilst the second prototype will be referred to as PCB based Chest Unit version 2 (PCU_v2). The aim of PCU_v1 is that of verifying the hardware implementation of each subsystem whilst using a small footprint. On the other hand, PCU_v2 is designed so as to have a system that is configurable to a particular set of specifications. These are determined by: the number of optrodes and their characteristics, the cable's characteristics, and a number of changes in the interface itself.

4.1 Voltage Generation and Power Delivery Architecture

Different methods for delivering dynamic power through an implanted cable have been reported in the literature [14] [16]. Power regulation typically occurs within the PI units, employing either DC/DC converters and/or linear voltage regulators. For systems using DC/DC converters (Figure 4.1(a)) it is possible to generate boosted supply voltages; albeit sacrificing current supply and increasing complexity (silicon area and/or off-chip discrete components). Using linear regulators, on the other hand, provides a simple, compact solution at the expense of efficiency. Furthermore, it is essential to provide a significantly higher voltage level to compensate for the regulator's drop (Figure 4.1(b)). Both methods require additional circuitry at the PI module, increasing area and adding to the inevitable IR loss on the wires of the communication channel.

This author however, proposes a new method that mitigates the need to coarse regulation within the PI modules, by instead adaptively regulating the power within the CI unit through closed-loop feedback. By continually sensing the current flowing through the implantable cable, the IR drop across the cable can be calculated (Figure 4.1(c)) and compensated for. The CI output voltage V_{DOWN} can subsequently be dynamically

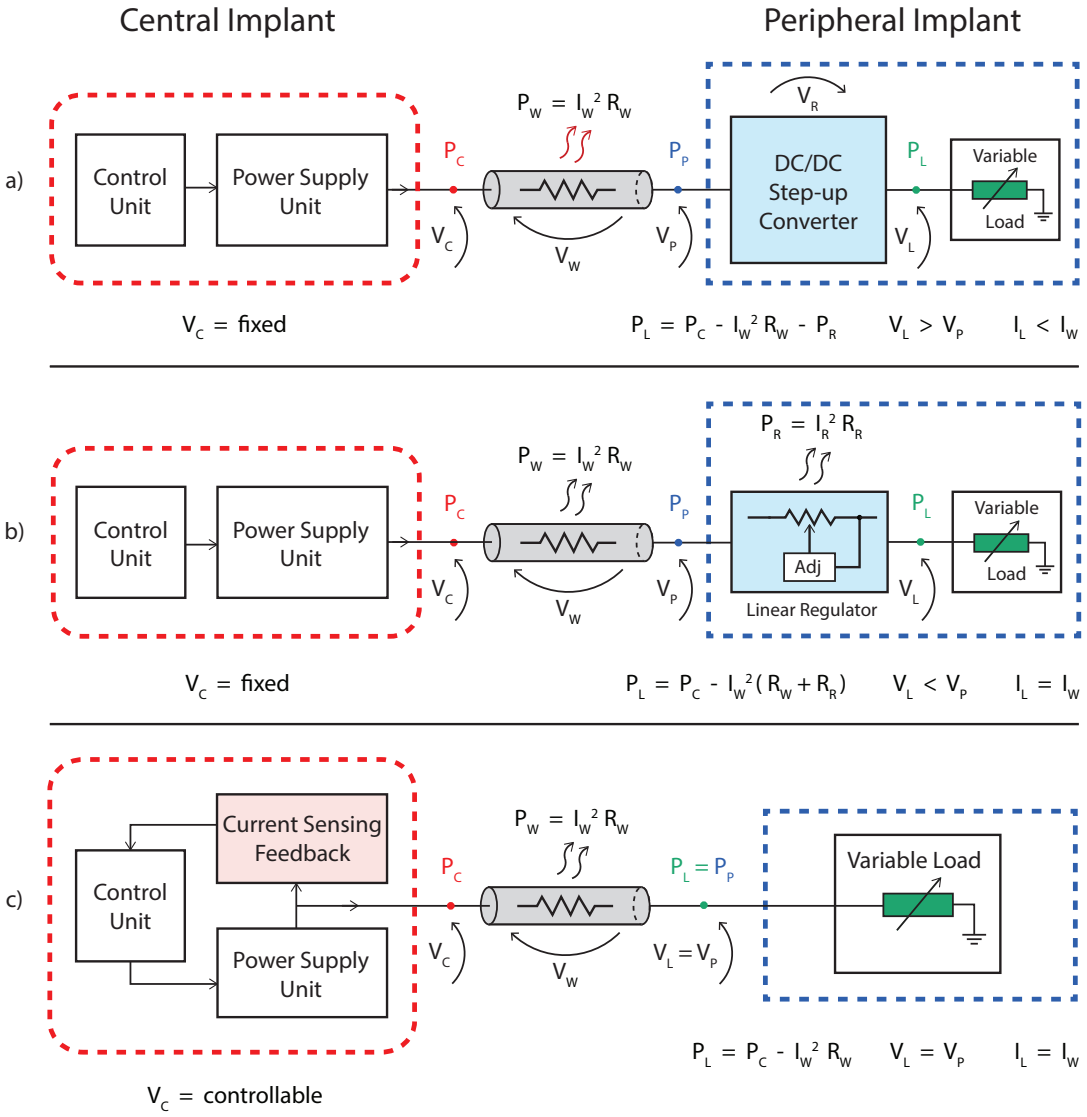


Figure 4.1: Three methods for power delivery, utilising (a) DC/DC conversion; (b) linear regulation; (c) adaptive, closed-loop regulation.

adjusted, based on the instantaneous load, I_{DOWN}, to ensure that a constant voltage level is received at the PI modules. As a result, the power loss in the delivery process is exclusively due to the IR drop across the wired link. This can easily be extended to multiple identical PI modules, provided that such modules have similar load characteristics. In this case, the current measured by the feedback path corresponds to the sum of the load currents of all the PIs; with the voltage received being common to all units.

4.2 Overall System Architecture

The system is divided into two PCBs which are, (1) the system controller and (2) a custom made PCB, used to implement the remaining subsystems. This was done in order to use the time allocated for this project for focusing on the design of the downlink driver, uplink receiver, and voltage generation subsystems; and to ease the implementation process.

To ensure compatibility with other developments in the CANDO project, the system controller is implemented by using an off the shelf development board, the IGLOO nano starter kit. This board contains a Microsemi AGLN250 Field Programmable Gate Array (FPGA), as presented in Figure 4.2. FPGAs have been around since 1986, with the basic blocks that make up such a device being: *logic blocks* containing several gates, flip-flops and memory (such as RAM), *programmable interconnect* providing a path for the required connections between various components to be made, and *Input/Output (I/O) blocks* providing an interface between external devices and internal logic of the FPGA. Such a device is programmed using VHSIC Hardware Description Language (VHDL); a hardware descriptive language that describes the logic/memory needed to perform the required function/s. The biggest advantage of using FPGAs is parallelism, as multiple functions can be executed simultaneously. For instance, in this project, some of these functions are the downlink and uplink communication.

On the other hand, the process of designing and testing the custom PCB will be described in the remaining sections and chapters.

4.3 Downlink Driver

As highlighted previously, the power delivery architecture that was chosen makes use of closed loop control. This method requires a measure of the current flowing through the implantable cable so that the downlink voltage, V_{down} can be changed accordingly. This is implemented by the current feedback system mentioned later in this Chapter.

The downlink driver is responsible for sending a square wave signal to the PMs (being the optrodes) providing power (as this is done differentially) and a data signal

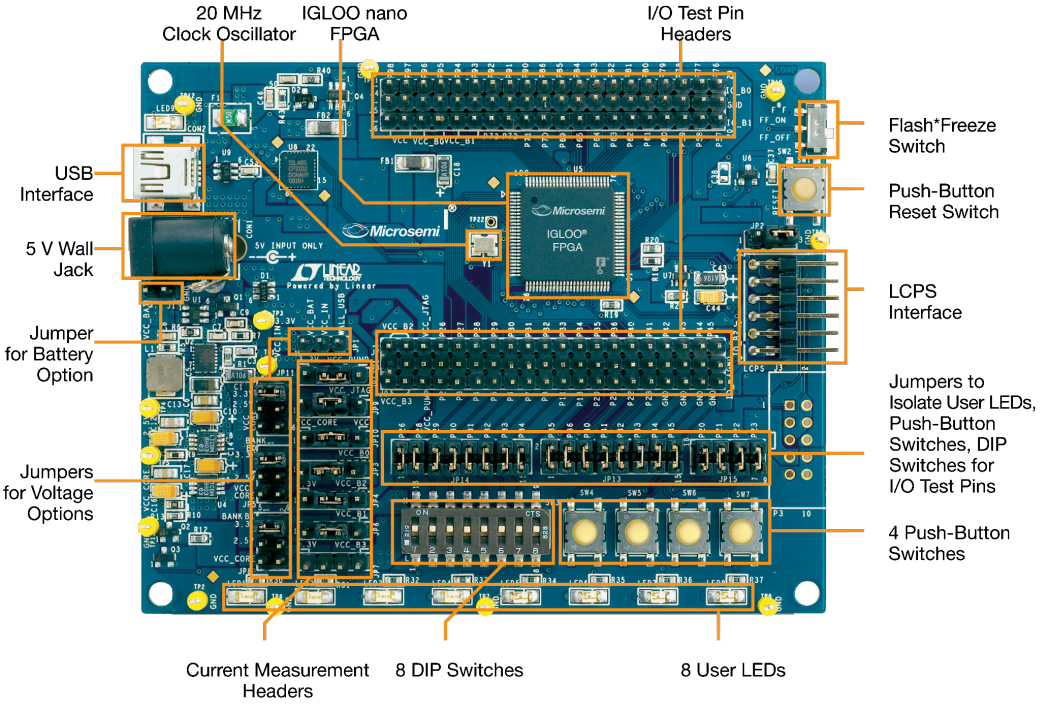


Figure 4.2: The IGLOO nano starter kit development board [20].

(using phase encoding). To keep a specific voltage (5V) at the output of the rectifier of the PMs, the voltage drops of the wired link and that of the rectifier need to be compensated for. Thus Equation 4.1 was used to derive the maximum (Eqn. 4.2) and minimum (Eqn. 4.3) voltages required by the downlink driver.

$$V_{down} = 5\,V + I_{down}R_{wire} + V_{rectifier\ drop} \tag{4.1}$$

$$V_{down_{MAX}} = 5\,V + (21.6\,mA \times 310\,\Omega) + 1.15\,V \quad = 12.85\,V \tag{4.2}$$

$$V_{down_{MIN}} = 5\,V + 1.15\,V \quad = 1.15\,V \tag{4.3}$$

In the Equation above, $R_{wire} = 2.2\,\Omega\,\mathrm{cm}^{-1} \times 2 \times 77\,\mathrm{cm}$ and I_{down} is the total quiescent current for 16 optrodes (0.2 mA×16), summed up with the total stimulating current for 8 optrodes (2.3 mA×8). PCU_v1 is however, designed for a 50 cm Cooper cable (since the 77 cm cable was not yet available, the maximum length as set in [19] ≈50 cm was used), a 1 V rectifier drop (as measured results were not available at the time), and a 2 mA stimulating current (not 2.3 mA). Therefore, the range of minimum and maximum voltages used for PCU_v1 is 6 V and 10.5 V respectively. A summary of the specifications

for this device are set in Table 4.1.

Table 4.1: Specifications for the downlink driver.

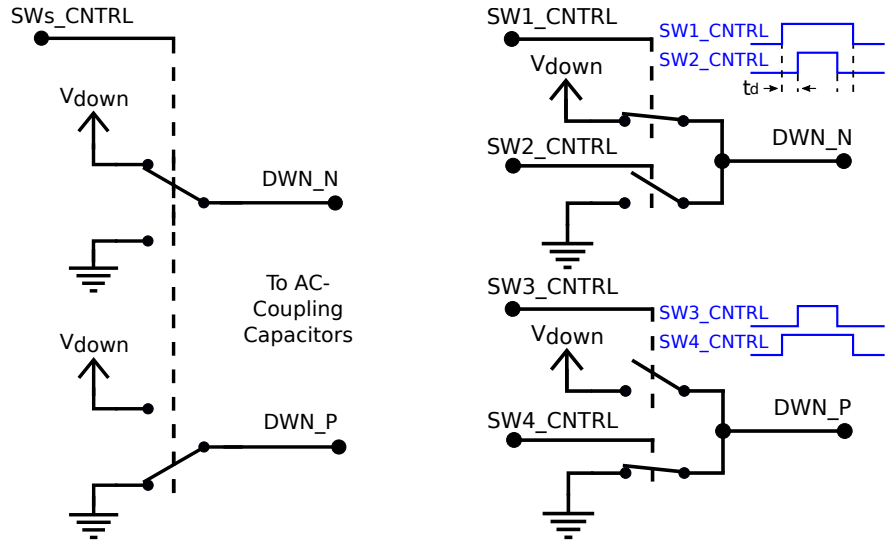
Feature	Specification
Minimum Voltage	6 V
Maximum Voltage	10.5 V
Single/Dual Supply	Single Supply
Switching Rate	>200 kHz
Rise Time/Fall time	<250 ns
Efficiency	>80 %
Maximum Current	>25 mA

Once the specifications were set, a decision was taken to construct the architecture of the driver out of two Single-Pole, Double-Throw (SPDT) switches as depicted by Figure 4.3a. This is because switches consume minimal static power (mostly due to leakage currents), and they can have a low on-state resistance; thus providing a very efficient solution when compared to using op-amp buffers. Switches in the SPDT configuration however, suffer from a high dynamic power dissipation due to the high current flowing during switch transitions (momentarily, both switches will be on). This can be reduced by implementing an SPDT switch using two Single-Pole, Single-Throw (SPST) switches (one Normally Open (NO) and the other Normally Closed (NC)); thereby ensuring that one switch is off before the other one is turned on. If this does not suffice, one can deliberately increase this delay, t_d (also known as the break-before-make-delay/dead-time) as illustrated in Figure 4.3b.

4.3.1 Downlink Driver – Component Selection

For the downlink driver, this author researched for SPST switches based on the specifications set in Table 4.1. These switches were then compared with each others characteristics as shown in Table 4.2.

As a result, MAX4679 was chosen as the downlink driver due to its low on-state resistance when compared to DG9426E. Even though ADC1613 has lower on-state resistance than MAX4679, the quiescent current of the chip increases if the digital interface does not swing up to the switch's supply. This effect is undesirable, and a way into reducing the current consumption would be to use a level translator to translate a 3.3 V/5 V



(a) SPDT configuration for the downlink driver.

(b) SPST configuration for the downlink driver.

Figure 4.3: Different configurations for the downlink driver.

digital signal to the required voltage. However, this solution increases the area occupied by the driver, and does not cancel out all the current consumption (as the level translator will also have a static current).

It is important to note that all these switch Integrated Circuits (ICs) are available in the same package, that is, TSSOP-16. Additionally, the pinout is very similar (the only difference is that the position of NO and NC switches may be swapped, and ADG1613 does not have a logic supply). Therefore, if on-state resistance is not the highest priority, but transition time is (or maybe signal swing), then DG9426E/MAX4663 can be soldered instead of MAX4679.

4.3.2 Downlink Driver – Schematic and PCB Design

[21] suggests that for power sequencing, analogue supply should be sequenced first, followed by the logic supply. As this is not possible in this application (unless extra circuitry is added to do so), a schottky diode needs to be inserted between the logic supply and analogue supply. Hence, a schottky diode with a low forward voltage was chosen and used in the design.

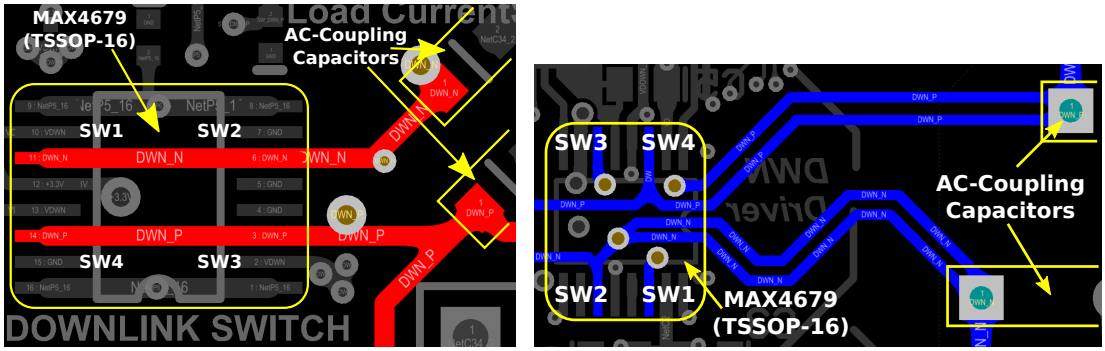
With respect to the PCB design, since two prototypes were implemented, the results

Table 4.2: SPST switch selection table. [■ Best ■ Worst]

Device	MAX4679	DG9426E	ADG1613	MAX4663
Type	2 NC, 2 NO	2 NC, 2 NO	2 NC, 2 NO	2 NC, 2 NO
Supply range (V)	2.7 – 11	2.7 – 16	3.3 – 16	4.5 – 36
Max. Supply current (µA)	1 - analog; 1 - logic	1 - analog; 1 - logic	1 - analog; 1 - logic *	0.5 - analog; 0.5 - logic
Max. leakage current per switch (nA)	±10	±10	±10	±5
Max. continuous current through switch (mA)	±100	±100	±140	±200
Typ. On-state resistance (Ω)	1.8 @ 5 V	3.1 @ 5 V	1.7 @ 5 V	3 @ 12 V
Typ. Rise Time (ns)	600 @ 5 V	62 @ 5 V	215 @ 5 V	200 @ 12 V
Typ. Fall Time (ns)	120 @ 5 V	29 @ 5 V	115 @ 5 V	100 @ 12 V

* Current increases to a max. of 480 µA if digital interface does not swing up to switch supply.

from the first served to make improvements on the second one. Thus, to decrease the dynamic power dissipation of the switches in PCU_v2, the outputs of the switches were shorted out at the AC-coupling capacitors (Figure 4.4b) and not at the pins of the switch (Figure 4.4a) itself. This maintains the resistance between one switch and the capacitor the same, but doubles that between the high-side (connected to V_{DOWN}) and the low side (connected to ground) switches. As a result, the current during switch transitions decreases; thereby decreasing dynamic power dissipation. Additionally, in order to ensure that the switch control signals are synchronised (and therefore 'arriving' at the same time at the switch's inputs), the lengths of their tracks were matched to the nearest 1 mm by using serpentine routing as depicted in Figure 4.5.



(a) Downlink driver routing for PCU_v1. **(b) Downlink driver routing for PCU_v2.**

Figure 4.4: Downlink driver routing for both PCB versions.

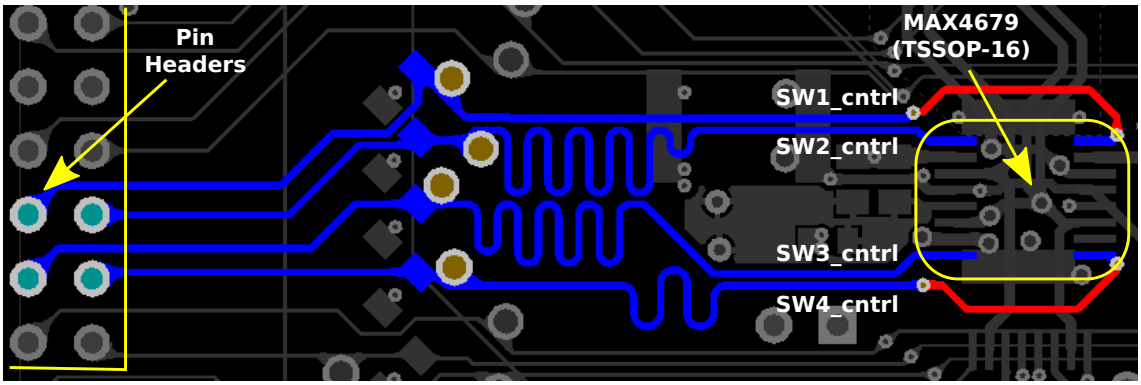


Figure 4.5: Serpentine routing used to length match control signals for the downlink driver.

4.4 Current Feedback System

For closed loop voltage control, the current flowing through the Cooper cable needs to be measured. Typical circuits for current measurements employ a current sensing resistor, R_{sense}, [22], ranging from a few mΩ to tens of ohms, depending on the current's magnitude. However, using such method increases the power losses by IR_{sense}. Therefore, in order to avoid additional components in the current's path, this author decided to use the on-state resistance of the SPST switches to measure the current. The on-state resistance however, changes for different supply and input voltages, as illustrated in Figure 4.6. As a result, the measurement will not be as accurate as when a current sensing resistor is used.

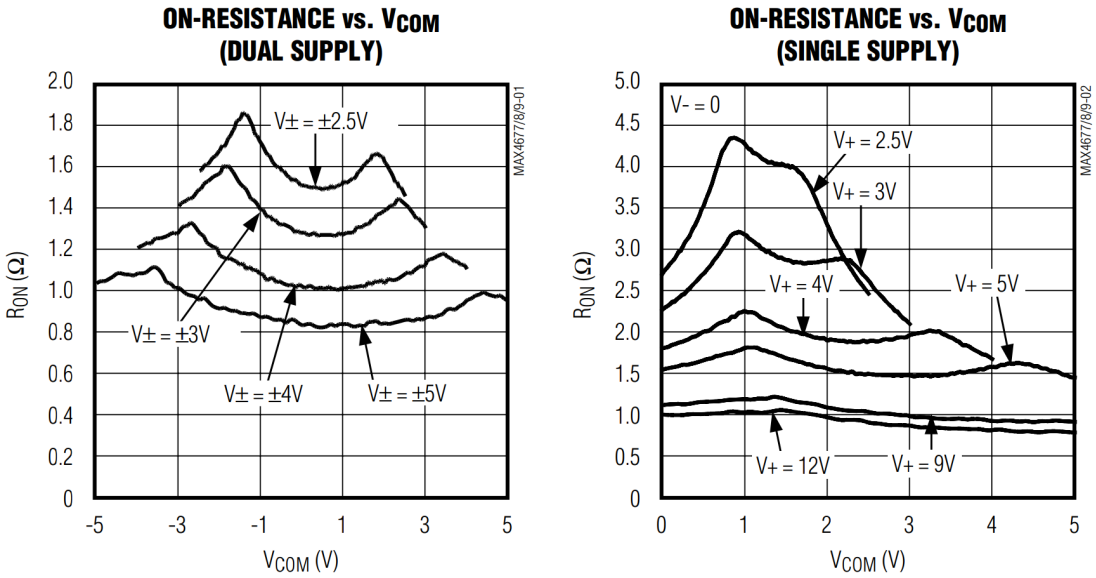
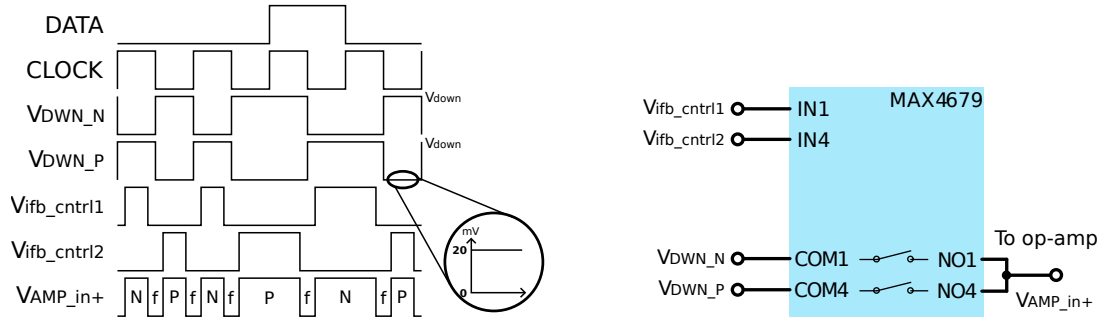


Figure 4.6: Switch on-state resistance (R_{ON}) against supply (V_+) and input voltages (V_{COM}).

When the maximum current of 20 mA flows through the switch, having a resistance of approximately 1.8 Ω, the resulting voltage drop on the switch is 36 mV. As this is too small for an Analogue to Digital Converter (ADC) to read, an amplifier is required to make use of the full input range of the ADC. Furthermore, since the driver's output pin is continuously switching between V_{DOWN} and ground, another switch is required to select between DWN_N and DWN_P, as displayed in the timing diagram of Figure 4.7a. This ensures that only the 'ground' signal is forwarded to the input of the op-amp (since V_{DOWN}>3.3 V), hence implementing low side current sensing. To make the PCB design easier, and at the same time keep compatibility, the same switch IC as the downlink driver is used between DWN_N and DWN_P as depicted in Figure 4.7b.



(a) Timing Diagram for Current feedback switch; *f* – floating; N – DWN_N; P – DWN_P.

(b) Switch circuit for current feedback system.

Figure 4.7: Switch circuit and its timing diagram for the current feedback system.

Thus the specifications of the amplifier were derived, as shown in Table 4.3. For the frequency response of the amplifier, a minimum pulse width of 1 ms was taken from [23] for the stimulation time of the Light Emitting Diodes (LEDs). Therefore, a bandwidth of 1 kHz is required, resulting in a minimum gain bandwidth product of 100 kHz.

Table 4.3: Specifications for the operational amplifier.

Feature	Specification
Supply Voltage	FPGA board works at 3.3 V.
Supply Current	<50 µA
Input Bias Current	<1 nA
Input Offset Voltage	<1 mV
Input Voltage Noise Density	Low
Rail-to-Rail Output?	Yes
Gain Bandwidth Product	>100 kHz
Open Loop Gain	>40 dB

4.4.1 Current Feedback System – Component Selection

Taking into consideration the specifications listed in Table 4.3, a search for an amplifier was carried out. As a result, four op-amps were identified as shown in Table 4.4.

Table 4.4: Operational amplifier selection table. [■ Best ■ Worst]

Device	MAX9913	OP281	TLV27L1	MAX417
Max. Supply Current (µA)	9	4	11	1.2
Typ. Input Bias Current (pA)	±1	3000	1	<0.1
Typ. Input Offset Voltage (mV)	±0.2	1.5	0.5	1
Input Voltage Noise Density ($nV/\sqrt{Hz}$)	400	75	89	150
Rail-to-Rail Output?	Yes	Yes	Yes*	Yes
Slew Rate (V/µs)	0.1	0.025	0.06	0.08
Gain Bandwidth Product (kHz)	200	95	160	80 – 150
Open Loop Gain (dB)	110	60	110	60

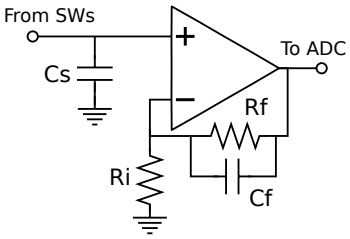
* not as good as others – swing from rail is 160 mV for a 2.7 V supply and 100 µA load.

Due to its high slew rate and bandwidth, and low input offset voltage, the MAX9913 operational amplifier was selected. It is important to note however, that this op-amp has a high input voltage noise density when compared with the remaining devices. Hence, it is imperative that any other noise contributions are minimised.

4.4.2 Current Feedback System – Schematic Design

For a non-inverting amplifier, the op-amp needs to be configured as shown in Figure 4.8a. To minimise additional noise contributions, resistors R_f and R_i have to be scaled so as to ensure that their contribution is minimal. Thus, once the gain was set, the resistor's values were calculated to ensure that their noise contribution is negligible, as tabulated in Table 4.8b. A capacitor, C_f, is also connected in the feedback path so that the amplifier behaves also as an integrator; filtering out high frequency components at the input (also acting as an anti-aliasing filter for the ADC). Its value (1.3 nF) was calculated so as to ensure that when the resistor, R_f (comprising of a potentiometer and a resistor in series) is at its maximum, the cut-off frequency of the integrator is 2 kHz.

Another thing to consider in this design is the fact that during operation, the node V_+ will either be equal to the voltage drop across the switches, or floating, since the multiplexer (selecting the line connected to ground) will be off as shown in Figure 4.7a.



(a) Amplifier circuit

Component	Ri	Rf	Op-amp
Value	280 Ω	Max. 60 kΩ†	N/A
Noise Density (V^2/Hz)	4.6 a*	994 a*	0.16 p

* calculated using $V_{nR}{}^2$=4kTR; † a rheostat

(b) Amplifier's noise analysis

Figure 4.8: Amplifier circuit and its noise analysis.

Therefore to keep the voltage at V_+ constant even when the node is floating, a capacitor (C_s) is connected across this node and ground. The value of this capacitor has to be low enough not to consume a lot of dynamic power and to ensure that it charges in the period of time during which the multiplexer is enabled. Also, it must be high enough to minimize droop due to leakage currents while the node is floating and due to switch charge injection (85 pC per switch).

Following the amplifier is an 8-bit ADC, MAX1118, which converts the analogue voltage to a digital bit stream. This is then sent to the FPGA via a Serial Peripheral Interface (SPI) with a maximum clock frequency of 5 MHz. This ADC has two multiplexed channels; one is used to monitor current, I_{DOWN}, whilst the other is used to monitor V_{DOWN} if necessary. The maximum bit rate this ADC can reach is 100 kSps.

4.5 Variable Power Supply

The downlink driver requires a variable power supply to adapt its driving voltage, V_{DOWN}, according to changes in the load. Such power supply can be implemented using either a DC/DC converter or a combination of a boost supply and a linear regulator.

A DC/DC converter is a switch mode power supply making use of switches (comprising of MOSFETs/BJTs) to switch the current flowing through an inductor between the input supply and the output supply. Such configuration is highly efficient (>75 %) at the expense of increased area. The higher the efficiency, the bigger the device will be, since most losses are due to a finite resistance in the inductor (reduced if cross-sectional area of the inductor is increased), and the on-state resistance of the switches (which decreases as

the area of the switch increases).

On the other hand, a linear regulator is a closed loop system which ensures a stable voltage at the output by varying the regulator's 'resistance'. This resistance will either be connected in series with the source, or in parallel, depending on the device. Hence, the regulator will dissipate the difference between the output and input voltages as heat. As a result, the efficiency of a linear regulator (≈60 %) is lower than that of a DC/DC converter. Contrary to the switching regulator, the area of a linear regulator can be made small as it is mostly designed using active components, and therefore does not require inductors.

For this project, a DC/DC converter was chosen, as efficiency was given the highest priority. Moreover, in the case of a linear regulator, a device to boost the voltage before the linear regulator would still have been required as the PCB is powered from a supply lower than V_{DOWN}. Thus, the selected configuration is that of a DC/DC converter with a programmable output voltage and a burst operating mode. Such mode enables the DC/DC converter to go to sleep during light loads, should the generated voltage be within specific thresholds. Once the voltage is below this threshold, the power supply will wake up, increase the voltage to the threshold, and go to sleep again. This is an effective way of reducing power consumption and increasing efficiency of the power supply.

4.5.1 DC/DC Converter – Component Selection

Based on the characteristics of the downlink driver, the specifications for the variable power supply were laid out, and a boost converter was selected from a number of available devices shown in Table 4.5. All these devices have a variable output voltage that is set by an external resistive divider (the centre of which is fed to the feedback pin of the device).

The device selected as a variable power supply is the LTC3130, due to its higher efficiency at light loads, low on-state resistance, and high switching frequency. To ensure that the downlink voltage stabilises within half a data bit (5 µs), it is imperative that the switching frequency is much higher than the downlink data rate.

Table 4.5: DC/DC converter specifications and selection. [■ Best ■ Worst]

Device	Spec.	LT3130	LT3129	TPS62770	LT1615
Input Voltage Range (V)	3.3-5	2.4-25	2.4-15	2.5-5.5	1.2-15
Output Voltage Range (V)	5-11	1-25	1.4-15.75	4.5-15	up to 34
Burst Mode Operation	Yes	Yes	Yes	Yes	Yes
Quiescent Current (µA)	<100	1.6	1.3	NA	20
Efficiency (%)	>80	87*	82*	75*	78⋆
Switching Frequency (MHz)	>1	1.2	1.2	1.05	NA
Maximum Load Current (mA)	>100	500†	200†	200†	<350
Switch On-state resistance (Ω)	<1	0.35	0.75	0.6	NA

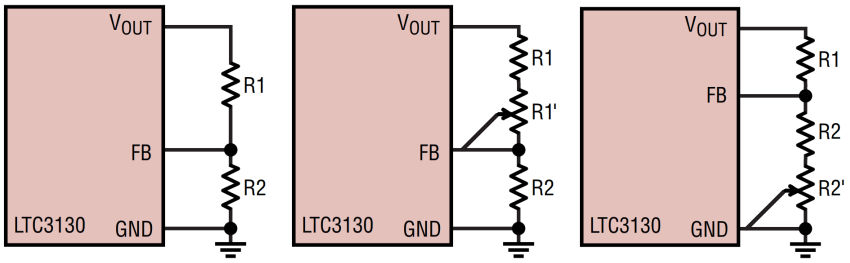
** 1 mA load current | * 5 V input, 12 V output | ⋆ 4.2 V input, 20 V output | † 5 V output

4.5.2 DC/DC Converter – Schematic Design

Unless integrated with the chip, a DC/DC converter requires an external inductor. The choice of this inductor depends on several factors including the recommended inductor and output capacitor values found in the datasheet [24] and the inductor's characteristics (equivalent series resistance, saturation current, size, and shielding). Keeping these factors in mind, this author chose a 10 µH, 92.4 mΩ, 4×4.1 mm inductor: the XAL4040-103.

Apart from the inductor, there is also a need to design the resistive divider connected to the chip which controls the output voltage of the boost converter. As mentioned earlier, this resistive divider has to be programmable so that the voltage at the output can be changed depending on the load. This can be implemented by making use of digital potentiometers (also referred to as digPOT in this thesis). However, keeping in mind that the design has to be low power and uses minimal area, the choice of a digital potentiometer presents several challenges.

According to [24], the voltage at the output follows Equation 4.4, whereby the node *FB* (see Figure 4.9a) is kept at 1 V. Hence, the output voltage can only be changed by varying either R_1' (Figure 4.9b) or R_2' (Figure 4.9c). Varying R_1' would give a linear relationship between the resistance and the output voltage. However, this would require a potentiometer that can sustain this quite high supply voltage (≈10 V). On the other hand, if R_2' is varied, the relationship between the resistance and voltage would no longer be linear. In this case, the voltage that the digPOT has to sustain will be less than 1 V.



$$V_{out} = 1 + \frac{R_1}{R_2} \quad (4.4)$$

(a) One time setting **(b) Varying R_1** **(c) Varying R_2**

Figure 4.9: Methods that can be used to vary the output voltage, V_{OUT} - which is also V_{DOWN} (Adapted from [24]).

Keeping this in mind the specifications for the digital potentiometer were set such that the resulting resistive divider:

1. Does not consume too much power – the end-to-end resistance of the potentiometer was set to 100 kΩ/200 kΩ), and to further decrease power consumption of the divider, multiple potentiometers are connected in series.
2. Occupies a small area – the footprint of the chip was given priority when deciding which device to choose.
3. Has a fast update rate – the interface was also given priority to ensure that the tap of the digital potentiometer settled as fast as possible to its tap position.

In view of this, it was decided to vary R_1' instead of R_2' as illustrated in Figure 4.9b. The reason being, that the footprint of these digital potentiometers tends to get bigger as the supply range increases to sustain a higher supply voltage range (10 V). Thus varying R_1' would only require a potentiometer working at the digital supply (3.3 V).

4.5.3 Digital Potentiometer – Component Selection

Based on these specifications, digPOTs were researched, gathering a combination of 100 kΩ and 200 kΩ potentiometers, as summarised in Table 4.6.

The MAX5161 was chosen as it occupies a small footprint with a very simple interface. On the other hand, the number of taps of this device is not much, and should this need to be increased, MAX5394 can be used. However, MAX5394 has an SPI interface, and should multiple devices be used, one can either apply one SPI module, and be limited

Table 4.6: Digital potentiometer selection table. [■ Best ■ Worst]

Device	MAX5161	AD5227	MAX5394	AD8402	MAX5424
No. of channels	1	1	1	2	1
Resistance, R (kΩ)	200	100	100	100	200
Footprint and Area	SOT6	TSOT-8	TDFN8	TSSOP14	TDFN8
(normalised to smallest and to R)	1.000	2.036	1.003	3.997	1.129
No. of Taps	32	64	256	256	256
Wiper Resistance (Ω)	400	100	200	200	325
Settling Time (µs)	1	1	0.66	18	1
Supply Current (µA)	0.6	0.4	0.6	0.01	0.5
Max. Interface Frequency (MHz)	7	50	50	50	5
Interface	Up/Down	Up/Down	SPI*	SPI†	SPI*

*† Requires N clock cycles to update the potentiometer; $\star$ N = 16; † N = 10;

to updating one digPOT at a time, or an SPI module for each digPOT (requiring a controller with multiple SPI modules).

4.5.4 Digital Potentiometer – Schematic Design

To reduce power consumption, three digPOTs in series are used, giving a total resistance of 600 kΩ. Hence, by applying the required voltage range, putting 600 kΩ as R_2' and re-arranging Equation 4.4 (to get Equations 4.5 and 4.6), the values for R_1 and R_2 can be calculated simultaneously for both PCB prototypes, as laid out in Table 4.7.

Table 4.7: Values for the resistive divider required by the DC/DC converter for V_{DOWN}.

Board	PCU_v1	PCU_v2
Required V_{low} (V)	6	6.15
Used V_{low} (V)	5.25	6
Required and used V_{high} (V)	10.5	10.9
R_1 (MΩ)	4.64	6.04
R_2 (kΩ)	487	619

$$V_{low} = 1 + \frac{R_1}{R_2 + 600\,\text{k}\Omega} \tag{4.5}$$

$$V_{high} = 1 + \frac{R_1}{R_2} \tag{4.6}$$

A lower V_{low} was used in both PCBs to cancel out possible variations in the end-to-end resistance of the digPOT. The resistance may vary between 150 kΩ and 250 kΩ (three in series would give a range between 450 kΩ and 750 kΩ) according to the datasheet of the digPOT. Whilst for PCU_v1 a worst case scenario was used, for PCU_v2, based on results obtained from the former, some small variations were applied. On the other hand, V_{high} was not changed as R_2' does not affect this value, as portrayed by Equation 4.6.

4.6 Additional Downlink Circuits

Apart from the main subsystem required by the downlink, other circuits where included in the design to ease the debugging process of the system, and to be able to monitor the system.

4.6.1 V_{DOWN} Monitoring

In both PCBs, one input channel of the ADC used is connected to the output of the current feedback system explained previously in Section 4.4. The other input channel is connected to an attenuator so as to be able to measure V_{DOWN}. On PCU_v1, this is implemented by using the node between R_2' and R_2 mentioned in the previous section, and amplifying the corresponding voltage by a certain gain to use the full input voltage range of the ADC. The gain depends on the resistor divider formed by the digPOTs and the resistor, R_2. For instance, for PCU_v1, the maximum voltage at that node is $1\,V \times (600\,k\Omega/(487\,k\Omega+600\,k\Omega))=0.552\,V$, whilst the minimum voltage will be ground (when digPOT is at $0\,\Omega$). Hence, in this case, an approximate gain of six is required. On the other hand, for PCU_v2, since resistors R_1 and R_2 are configurable, a specific gain would not work as this requires both resistors to be fixed. Thus in this case, a simple voltage divider between V_{DOWN} and ground is used to attenuate the voltage and feed this to the input of the ADC. This enables the user to monitor also V_{DOWN} from the GUI during system operation. However, the ADC's input will also load the resistive divider, resulting in an error in the final value of the ADC.

4.7 Uplink Receiver

Apart from chest to brain communication, the opposite is also required at a maximum bit rate of 1.6 Mbps. The challenge is recovering the digital data from the analogue signal received at the CI. This signal can have different characteristics depending on: the properties of the Cooper cable (especially the length, resistance and capacitance); the bit rate used (800 kbps/1.6 Mbps); the bit stream itself; and the characteristics of the

downlink interference on the uplink wires.

Before going into the design and implementation of the uplink data recovery, it is important to take a look at various waveforms that may be received at the CI, as illustrated in Figures 4.10 and 4.11. The ideal received differential uplink waveform should be a square wave with a peak-to-peak amplitude of 6 V. However, due to the capacitance of the Cooper cable, this is not the case. The capacitance is changing the behaviour of the line driver at the brain side from voltage mode to current mode. The triangular shape is due to the capacitance between the uplink and downlink wires being charged/discharged with a constant current. To reduce/remove this effect, the spacing between the downlink and uplink wires can be increased, in the process reducing the capacitance. This can be done by either changing the current configuration (used in [15]) of the conductors of the Cooper cable (to the one shown in Figure 4.12b) or by using a two-conductor Cooper cable for each link (one for uplink and one for downlink) as depicted in Figure 4.12c.

The capacitance for each wire in Figures 4.12a and 4.12b are calculated below. For Figure 4.12c, the capacitance between the uplink and downlink will be much smaller than that in (a) or (b), as the minimum spacing between these wires will approximately be the diameter of the cable.

Let the capacitance between two adjacent wires be denoted by C.

Configuration used in [25] (Figure 4.12a)

$$\begin{aligned} C_{U1} &= C_{U1D1} + C_{U1D2} \\ &= C + \frac{C}{2} &&= \frac{3C}{2} \\ C_{U2} &= C_{U2D1} + C_{U2D2} \\ &= \frac{C}{2} + C &&= \frac{3C}{2} \end{aligned}$$

New configuration (Figure 4.12b)

$$\begin{aligned} C_{U1} &= C_{U1D1} + C_{U1D2} \\ &= C + \frac{C}{2} &&= \frac{3C}{2} \\ C_{U2} &= C_{U2D1} + C_{U2D2} \\ &= \frac{C}{2} + \frac{C}{3} &&= \frac{5C}{6} \end{aligned}$$

Before interpreting the results above, lets take a moment to identify the role of the capacitance equalisation network. In the case where no capacitance equalisation network is connected to the system, $C_{UxD1} \neq C_{UxD2}$ (x can be 1 or 2). Therefore the coupling of

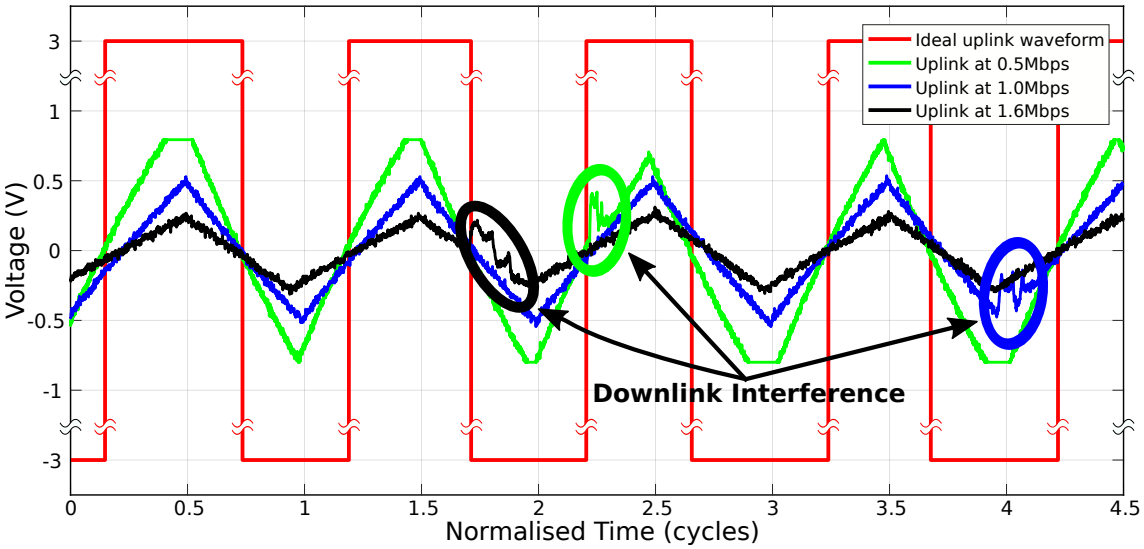


Figure 4.10: Uplink differential peak-to-peak voltage (received at the chest terminals) at different bit rates without a termination resistor.

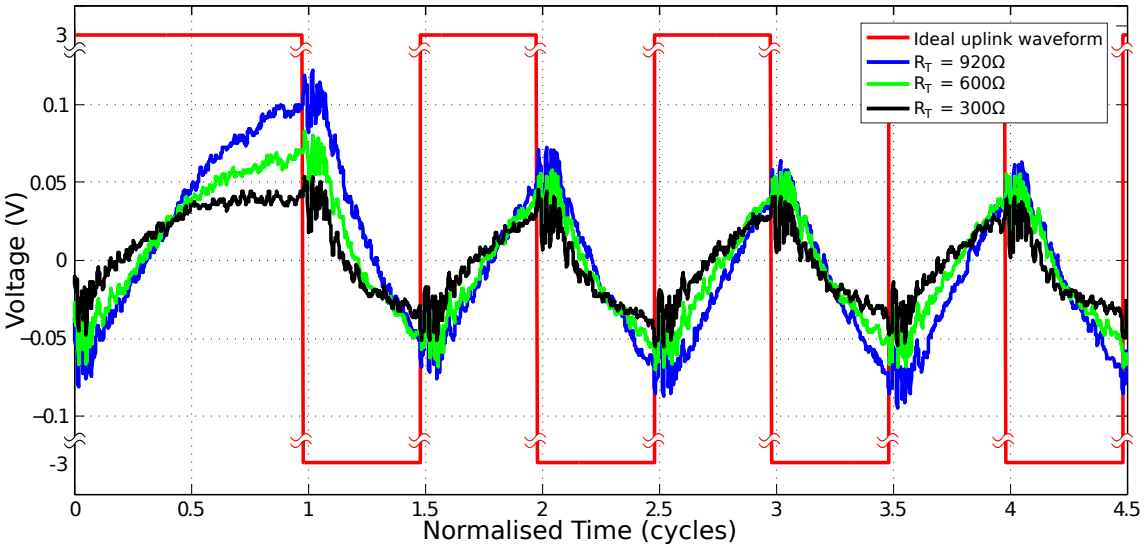
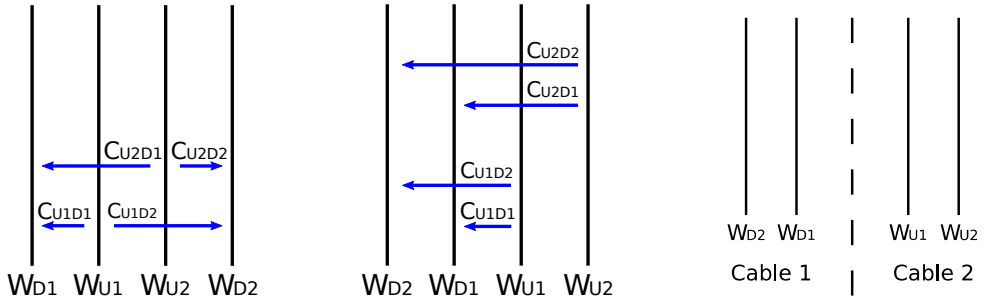


Figure 4.11: Uplink differential peak-to-peak voltage (received at the chest terminals) at 1.6 Mbps with different termination resistors.



(a) Configuration as used in [15].

(b) New Configuration using 1, 4-wire cable.

(c) Configuration using 2, 2-wire cables.

Figure 4.12: Decreasing the capacitance between the uplink and downlink wires; D1 and D2 refer to downlink wires, whilst U1 and U2 refer to uplink wires.

the downlink signals, D1 and D2 on the uplink wire Ux, will not be equal. As a result, a wave, similar in shape to either D1 or D2 (if $C_{UxD1} > C_{UxD2}$, then the waveform will be similar to that on D1 and vice versa - just a smaller amplitude) is present on the uplink wire Ux. To remove this coupling, there are three different cases to consider as follows:

1. Now, if one were to assume *ideal waveforms* for D1 and D2, such waveforms would: have the same peak-to-peak voltage, and be symmetrical; such that their rise time, t_r is equal to the fall time, t_f. In this case, to cancel out the coupling of D1 and D2 on any uplink wire, Ux, only matching of C_{UxD1} to C_{UxD2} is required. In doing so, the coupling from both downlink wires is equal at any point in time, hence eliminating the interference completely on each wire. On the other hand, if the waveforms are not ideal, the resulting voltage on the uplink wire will not cancel out.
2. If the signals on D1 and D2 have a *different peak-to-peak* voltage (but transition times are equal), the resulting waveform will be similar to the wire with the largest peak-to-peak voltage. Nonetheless, in order to cancel out this effect, one may further increase the capacitance connected to the least dominant downlink wire, that is, if the resulting waveform is similar to D1, C_{UxD2} needs to be increased to increase the effect of D2 on Ux hence, cancelling out the coupled waveform due to D1.
3. Similar to the previous scenario, if the signals on D1 and D2 have *different transition times*, the resulting waveform will have a non-zero value. This only happens during transition times as illustrated in Figure 4.13. Contrary to the previous scenario, this cannot be eliminated by adding an additional capacitance to C_{UxDx}. Yet, if the coupling of D1 on U1 is made equal to the coupling of D1 on U2, since the coupled waveform has the same exact characteristics (peak-to-peak voltage and transition time) on both wires, the resulting differential voltage across both U1 and U2 due to D1 will be zero. If the same is applied to D2, the net differential voltage across U1 and U2 should be zero. However the voltage on each wire will not be zero.

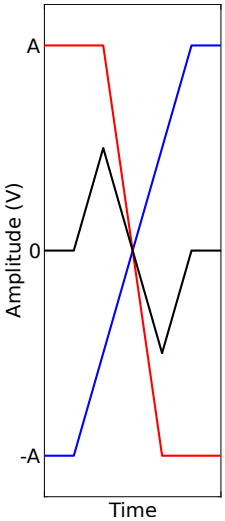


Figure 4.13: The effect of asymmetrical transition times on the signal coupled on the uplink wire/s.

Back to the results obtained for Figures 4.12c and 4.12b, the capacitance equalisation network for (b) will require a capacitor equal to C/2 for C_{U1D2} (to make it equal to C_{U1D1}), and a smaller capacitor for C_{U2D2}, as C/3 needs to be equalised to C/2. This however, applies to scenarios (1) and (2) listed above. Should transition times be mismatched, the capacitance equalisation network will not change from configuration (a) to (b).

On the other hand, should a termination resistor be connected at the chest side across the uplink wires, the capacitance equalisation network is not required any more. This is because when there is no activity on the line, the voltage induced from the downlink on the uplink wires can be dissipated in this resistance. However, using a termination resistor also changes the amplitude and shape of the uplink when data is being sent to the CI, as shown in Figure 4.11. This reduction in amplitude limits the amount of hysteresis that can be applied to the signal to ensure a smooth, glitch free output from the comparator. Hence, all these variables had to be kept in mind when choosing, and designing the circuitry required in order to change the waveform received at the CI to a digital signal.

Another significant aspect is that for configuration (b), one of the uplink wires (U2) has nearly half the capacitance than in configuration (a). Theoretically, for the same current, the slew rate for that wire should increase, reaching a higher voltage.

4.7.1 Architecture Selection

There are a number of subsystem architectures that were considered for uplink circuitry as illustrated in Figure 4.14. These architectures will be described and comparisons made, showing the advantages and disadvantages of each one. For all these architectures, the downlink glitches may be reduced by placing a low pass filter between the analogue circuitry and the comparative device. Such glitches are similar to a narrow pulse (in shape) and appear during the transition of the downlink.

(a) *A comparator with hysteresis* – This is one of the simplest architectures that can be used to convert the analogue signal into a digital one. Hysteresis is applied by

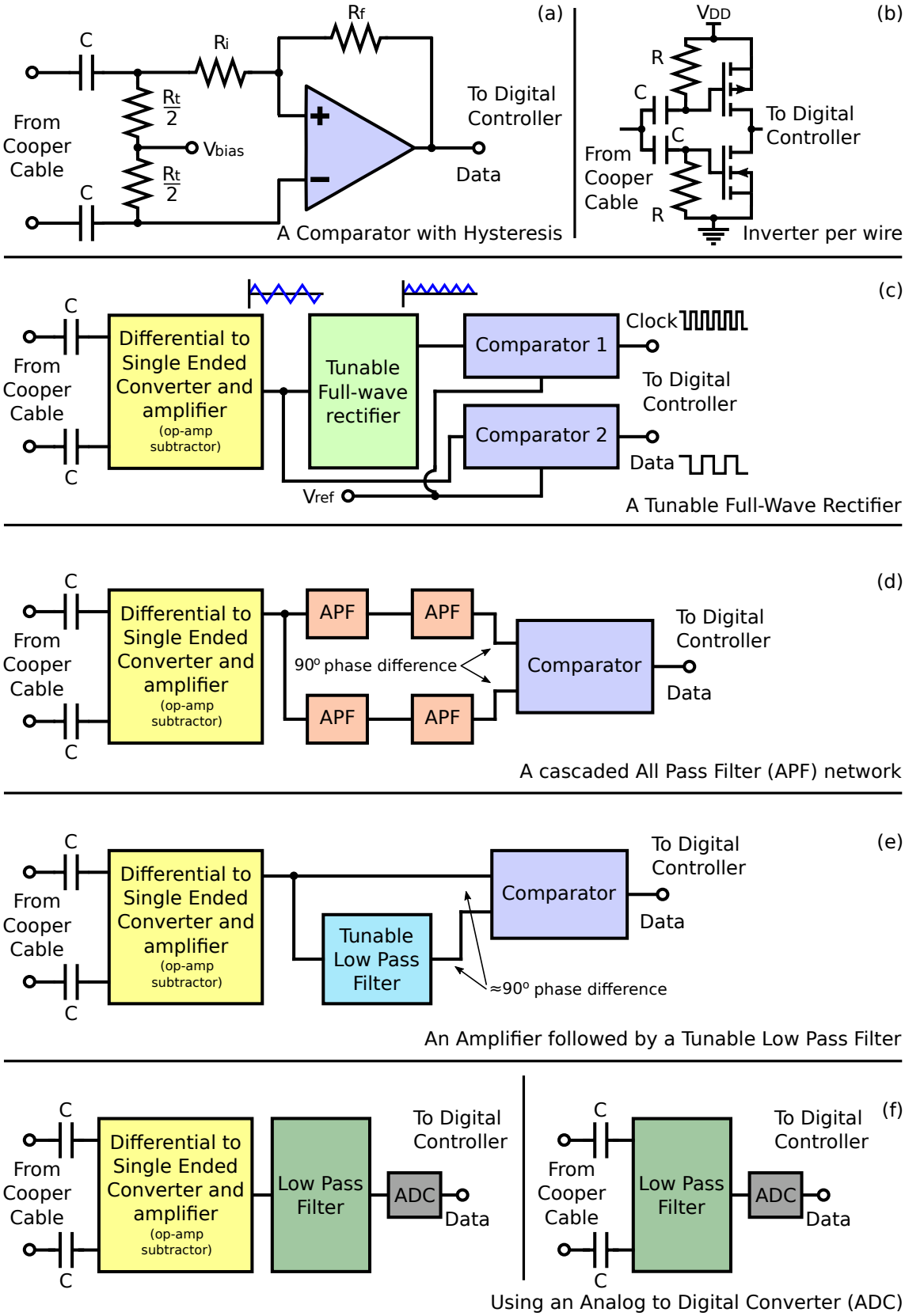


Figure 4.14: Six different uplink configurations.

using positive feedback using R_f and R_i. However, should the downlink glitches be of the same amplitude as the uplink signal, the comparator will not 'differentiate' between the two, and therefore these glitches will also appear at the output of the comparator.

(b) *An inverter for each wire* – A very basic circuit, which thresholds the signal arriving at the CI (no hysteresis). Such circuit requires a higher signal swing than the comparator due to V_{th} of the MOSFETs. Additionally, the signal received needs to be a square wave to ensure that the pulse width is correctly level shifted at the output of the inverter. Such configuration uses the least amount of power and occupies the least amount of area.

(c) *A tunable full-wave rectifier* – The idea behind this circuit is to use the properties of a triangular waveform to recover both a clock signal and the data from the uplink signal. This is done by rectifying the waveform so that the negative part is put with the positive part, and thus a clock dependent on the data can be derived from the signal. This architecture, however, works only should the waveform have no offset (or a constant offset). If the offset changes during operation, such architecture cannot be used (or ways to cancel that offset need to be identified).

(d) *A cascaded all pass filter network* – As the name implies, in phase encoding, data is encoded in the phase of the signal. Thus, the phase of such signal (and therefore even pulse width) is important as this conveys the information needed. Hence, the data can also be recovered by phase shifting the required frequency spectrum (the data/triangular waveform) by 90^o in phase, whilst keeping the rest (downlink glitches) at the same angle. This, and the phase shifted version, are then fed to a comparator, and the digital signal is obtained containing data that is free of downlink glitches. However, multiple all pass filters are required to get a differential phase shift of 90^o between a network of filters, thereby occupying a significant amount of area. The design of these networks is simplified through the use of normalisation tables according to filter order and acceptable phase error as found in [26].

(e) *An amplifier followed by a tunable Low Pass Filter (LPF)* – This architecture uses the same idea in (d), but focuses on reducing component count, leading to a reduction

in area. Since the number of data rates that can be used by the uplink are finite, it is possible to replace the network of all pass filters to a simple low pass filter. This is tuned at the set data rate, giving a certain phase shift (depending on the order of the filter). Therefore by knowing the data rate beforehand (or if circuitry is fast enough, even in real time), the low pass filter can be tuned to a specific frequency.

(f) *Using an ADC* – Contrary to the above-mentioned architectures whereby the uplink was converted into a digital signal by using analogue circuitry, this architecture uses an ADC instead. This ADC digitises the analogue waveform, so that the controller can recover the data using digital processing. However, such architecture may use a significant amount of area and power.

In order to choose an appropriate architecture, all architectures were compared as depicted in Table 4.8. As a result, architecture (e) was deemed to be a good balance between power, area, and offset and downlink interference sensitivity. However, since such configuration requires also a comparator, it was decided to design the system in such a way, that one can choose to use either architecture (a) or (e), depending on the properties of the uplink waveform received. It is also worth noting that for PCU_v1, architecture (b) was used since at the time, the results from uplink testing were not yet available, and therefore ideal waveforms were considered.

Table 4.8: Comparison of uplink architectures.

Architecture	(a)	(b)	(c)	(d)	(e)	(f)
Power	5	6	3	2	4	1
Area	5	6	3	1	4	2
Downlink Interference	2	1	3	6	5	4
Offset in Uplink	2	1	3	6	5	4
Total	14	14	12	15	18	11

$6 \rightarrow 1$; best $\rightarrow$ worst.

Based on this architecture, a comparator, and an op-amp (for the op-amp subtractor, and possibly for an active LPF) had to be selected. This author researched such devices, and useful ICs, and their properties were tabulated as shown in Tables 4.9 and 4.10. With regards to PCU_v1, FDG6320C (a chip with two MOSFETs: 1 PMOS and 1 NMOS), with a V_{TH} of $\pm 0.85\,V$ was used to form the circuit depicted in Figure 4.14(b).

Table 4.9: Comparator selection table. [■ Best ■ Worst]

Device	ADCMP609	TLV3201	LMV7239	LTC6702	MAX987
Typ. Input Offset Voltage (mV)	±3	1	0.8	1	±0.5
Typ. Internal Hysteresis (mV)	0.1	1.2	NA	4.3	±2.5
Differential Input Impedance (Ω)	200 k - 7 M	10^{13}	BJT input	NA	NA
Typ. Supply Current (µA)	550	36	52	24	48
Typ. Rise Time (ns)	25 - 50	4.8	1.7	11*	15
Typ. Fall Time (ns)	25 - 50	5.2	1.7	15*	15
Variable Hysteresis	Adjustable*	External†	External†	External†	External†
Propagation Delay (ns)	40	40	96	320	210

*Maximum toggling rate is 3.2 MHz; * using a resistor; † using positive feedback

Table 4.10: Uplink operational amplifier selection table. [■ Best ■ Worst]

Device	OPA835	LMV651	LTC6261
Typ. Supply Current (µA)	245	115	245
Typ. Input bias current (nA)	200	80	60
Gain Bandwidth Product (MHz)	30	12	29
Slew Rate (V/μs)	120	3	7
0.1 % Settling Time (µs)	0.065	NA	0.3
Rail-to-Rail Output?	Yes	Yes	Yes

For the comparator, TLV3201 (2-channel version – TLV3202) was chosen due to its high input impedance, low propagation delay, and low transition times. Moreover, ADCMP609 was also used to check whether an adjustable hysteresis without using positive feedback can lead to better results, at the expense of increased power consumption, and longer transition times. On the other hand, OPA835 (2-channel version – OPA2835) was selected as an amplifier because of its high gain bandwidth product, high slew rate, and low settling time. A high gain bandwidth is desirable in case a gain higher than one is required (with a gain of 10, bandwidth =3 MHz).

4.7.2 Uplink Receiver Schematic Design

The following describes the auxiliary components required by each block in Figure 4.14(e):

- For the *op-amp subtractor*, a gain can be set by changing the ratio of the resistors used. Additionally, these resistors should have a high value to reduce power dissipation and not to load the uplink drivers. However, a high value of resistance in the feedback loop of the op-amp leads to a reduction in bandwidth due to interaction with circuit parasitic capacitances. Thus, a 10 kΩ resistor was used as the feedback

resistor; setting a gain of 10 (with 1 kΩ input resistor).

- The *tunable low pass filter* is implemented by a simple passive RC filter. Such filter has a low component count, and its cut-off frequency can be easily changed by adjusting either R or C. However, this implementation gives a phase lag of only 45° at the cut-off frequency and not the desired 90°. For this phase response, a second order filter is required. Unfortunately, a tunable second order filter would require the ability to adjust two components, doubling the occupied area and increasing system complexity.
- For the *comparator*, TLV3202, hysteresis was applied by using a multi-turn 25 kΩ potentiometer.
- Biasing at mid-supply is achieved by a buffered voltage divider. The op-amp used to buffer this signal is the MAX9913 (also used in the downlink current feedback system).

The final schematic is illustrated in Figure 4.15. The blocks were designed separately, so that each block can be put in the signal's path or removed (using pin headers and shunt jumpers), depending on the waveform of the uplink. The possible configurations are as follows:

1. For a square wave (with minimal downlink glitches), the comparator circuits (c) or (d) are connected to the uplink wires (with the AC coupling capacitors). The rest of the circuitry is powered off.
2. For waveforms with a small amplitude, the subtractor (f) is connected to the uplink.
   (a) If the glitches of the downlink are significant (compared to the uplink's amplitude), the subtractor's output, V_{sub_out}, is connected to the LPF's (b) input. The filter's output is then connected to the tunable LPF (a) and to the positive input of the comparator. The negative input of the comparator is connected to the output of the tunable LPF.
   (b) If downlink glitches are not as dominant, the subtractor's output is connected to the input of the tunable low pass filter (a), and to the comparator's positive input. The output of tunable low pass filter is connected to the negative input

of the comparator.

Both TLV3202 and ADCMP609 can be used as the comparator.

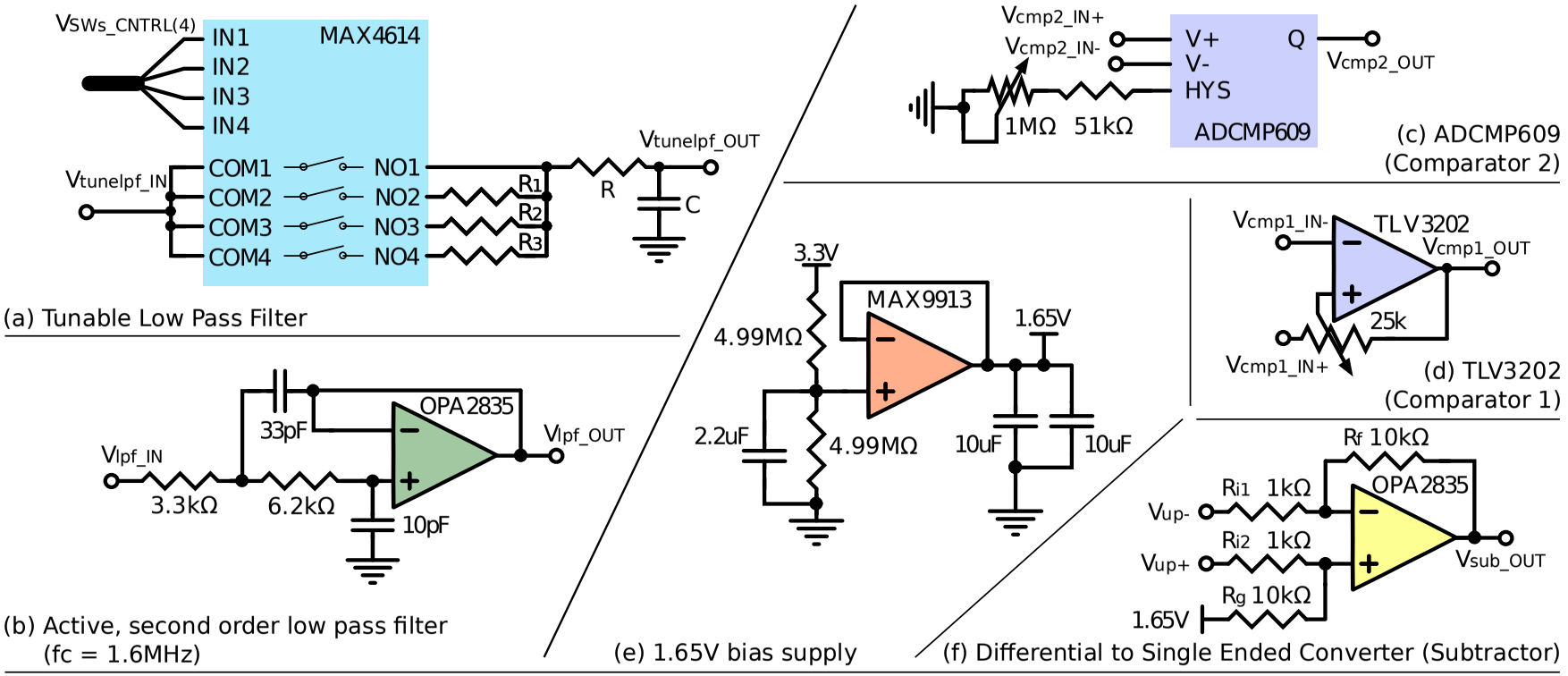
4.8 System Monitoring

Apart from the subsystems highlighted above, other circuits are included in PCU_v2 so as to facilitate system monitoring and debugging. These circuits include:

1. Two comparator circuits – one to check whether V_{DOWN} is greater than 11 V and the other to assert its output if I_{DOWN} is higher than a certain threshold set by a potentiometer.
2. LEDs – used to show visually the status of the 5 V, 3.3 V and V_{DOWN} power supplies –  . These are also used as an indicator should V_{DOWN} exceed 11 V (and therefore the downlink driver needs to be replaced with one that can handle this voltage), and similarly I_{DOWN} –  . Even though the used LEDs have a low power consumption (2 mA), a power-off switch is included in the design to ensure that they are not included in any current measurements (such as efficiency) that may be required.
3. A 4×4 breadboard – instead of using pin headers to connect the capacitance equalisation network and the 4-wire Cooper cable, a small breadboard is used as it is more practical and easier to handle.
4. A voltmeter – continuous supervision of V_{DOWN} is important, as it ensures that the system is operating as required. Therefore to decrease the amount of equipment needed to run and monitor such a system, a voltmeter was also considered in the design.

4.9 Printed Circuit Board Design

After designing all circuits, ensuring that all components have been selected, and are available from suppliers, PCB design was initiated. In both prototypes, the variable power supply, comprising of a switching DC/DC converter, was segregated from sensitive



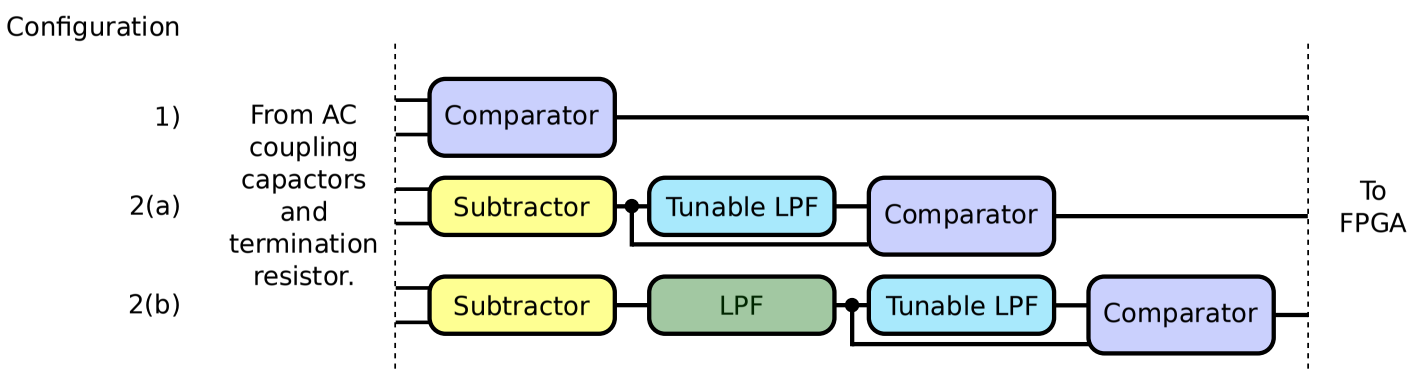


Figure 4.15: Uplink schematic

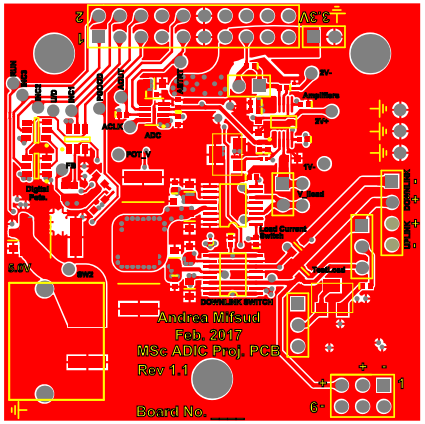
amplifier circuits (such as current measuring op-amp) to reduce any coupling between the circuits. Additionally, all digital pins were routed to one side of the PCB to make future integration of an FPGA on the board easier. Lastly, for PCU_v2, since more circuitry needed routing for the uplink part of the system, the design was split in two, such that downlink circuitry was routed on the bottom layer, whilst uplink circuitry was laid out on the top layer of the PCB.

The resulting PCBs are illustrated in Figure 4.16. Whilst PCU_v1 is a 5×5 cm, 2-layer PCB, PCU_v2 is a 10×10 cm, 4-layer PCB with internal ground and power planes.

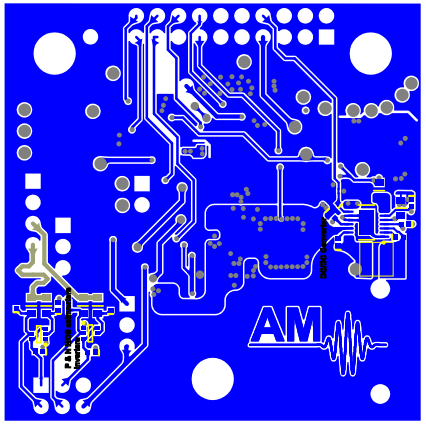
4.10 Summary

The design process for each subsystem has been described, starting off with a description of the technologies available. This was then followed by the component selection process, where the market was researched for potential devices. These devices and their characteristics were compared to the specifications set by the particular subsystem. One/multiple devices were selected, and the rationale behind such decision explained. Then the schematic design for this subsystem was described, designating the remaining components in the subsystem. Finally, if applicable, any PCB design techniques used in the implementation of this subsystem were highlighted, and such decision justified. A summary of the components that have been selected for each subsystem is available in Table 4.11.

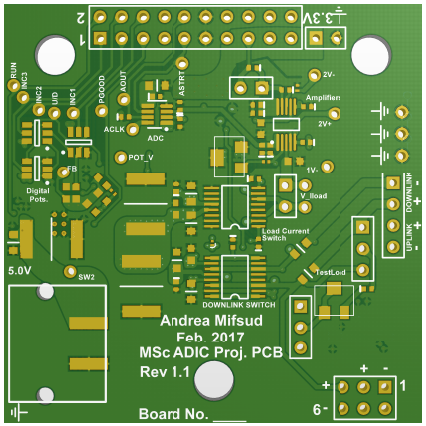
PCU v1 (5x5cm)



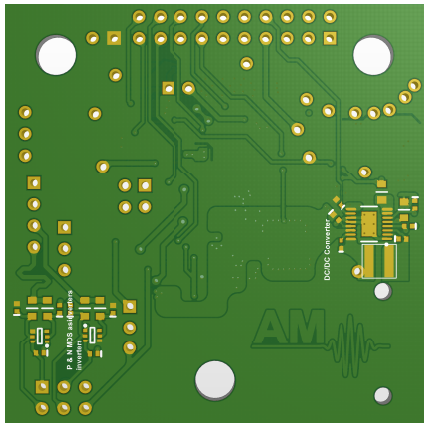
(a) Top Layer (with silkscreen)



(b) Bottom Layer (with silkscreen)

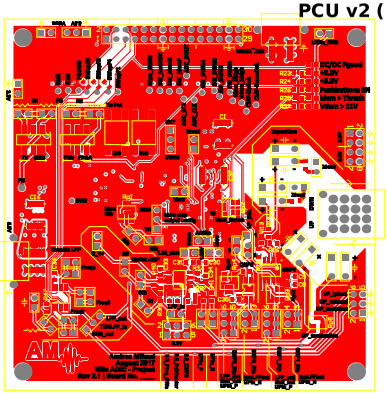


(c) 3D PCB Top (with solder mask)

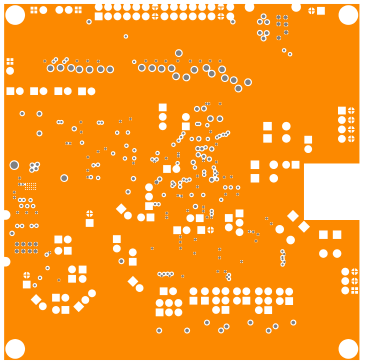


(d) 3D PCB Bottom (with solder mask)

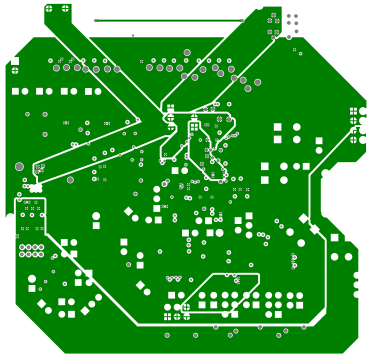
PCU v2 (10x10cm)



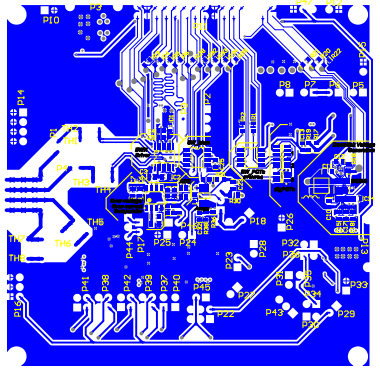
(e) Top Layer (with silkscreen)



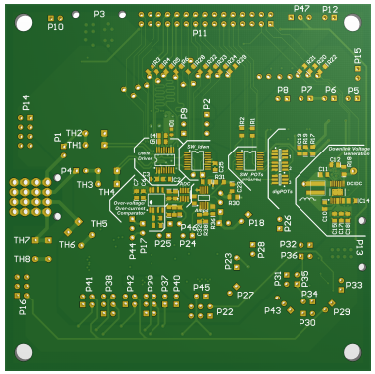
(f) Internal GND Plane



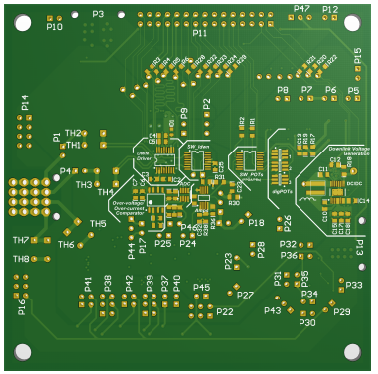
(g) Internal Power Plane



(h) Bottom Layer (with silkscreen)



(i) 3D PCB Top (with solder mask)



(j) 3D PCB Bottom (with solder mask)

Figure 4.16: 2D and 3D PCB views for both PCU_v1 and PCU_v2.

Table 4.11: Hardware Design - summary table

Function	*Component*
Downlink Driver	
Variable power supply	LTC3130
Digital potentiometer to vary V_{DOWN}	MAX5161
Downlink driver	MAX4679
Downlink Current Feedback System	
Downlink ground multiplexer for I_{DOWN} sensing	MAX4679
Current feedback op-amp amplifier	MAX9913
Current feedback ADC	MAX1118
Uplink Receiver	
Op-amp	OPA2835
Comparator 1	TLV3202
Comparator 2	ADCMP609
Switch array for Tunable LPF	MAX4614

Chapter 5

Software Design

FOLLOWING the design and implementation of the PCB, the firmware required for the system to operate had to be developed. This process was initiated whilst waiting for the PCBs to be manufactured; starting off with the FPGA's system and then, the GUI. Both of these are described and explained here in this section.[1]

5.1 FPGA Development

To facilitate the development of the FPGA system, this was divided into small modules as depicted in Figure 5.1. Each module has a specific function, as follows:

- *Downlink module* – controls the downlink switches such that the data is encoded in the power signal. It also controls the multiplexer switches that are used to select between DWN_N and DWN_P to measure the load current.
- *Power supply module* – keeps track and updates the digital potentiometers used to implement a variable power supply.
- *Current feedback module* – interfaces with the ADC and converts the obtained value to a count (the total number of taps by which the potentiometers need to be switched). This count is then used by the power supply module to update the digital potentiometers.

[1] Due to length constraints of this dissertation, the VHDL for the FPGA, and the block diagram for the LabVIEW GUI were not included. However, should this be required, one can email this author at am6416@ic.ac.uk

- *Uplink module* – decodes the uplink data received from the brain implant, and controls the tunable LPF.
- *Main controller module* – monitors the system to ensure correct operation, and interfaces with the GUI, decoding received commands, and sending any necessary data.

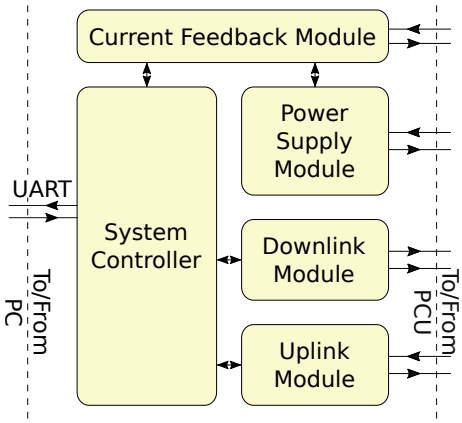


Figure 5.1: The FPGA subsystem divided into multiple modules.

The FPGA board used for this project has an input clock with a frequency of 20 MHz. Since this is not fast enough to run the controller module, a Phase Locked Loop (PLL) in the FPGA fabric is used to synthesize new clock signals with different frequencies. The chosen frequencies are 40 MHz, 5 MHz and 2 MHz.

5.1.1 The Downlink Module

The downlink interface has a data rate of 100 kbps, and therefore another clock signal needs to be generated from the available 2 MHz clock. This is done by using a counter, *main_count*, which restarts after reaching a specific value (in this case 19 - to divide the 2 MHz clock by 20 and get a 100 kHz clock). The data which is loaded by the user and then stored in a shift register is serially *XOR*'ed with this clock to phase encode the signal as required by the interface. In the event that a reduction in the dynamic power dissipation of the downlink switch drivers is desired, different signals (delayed by one 40 MHz clock cycle) can also be sent to the switches as shown in Figure 5.2. These signals have a dead-time of 1 clock cycle (25 ns using the 40 MHz clock).

Apart from the downlink drivers, this module has to send the appropriate signals

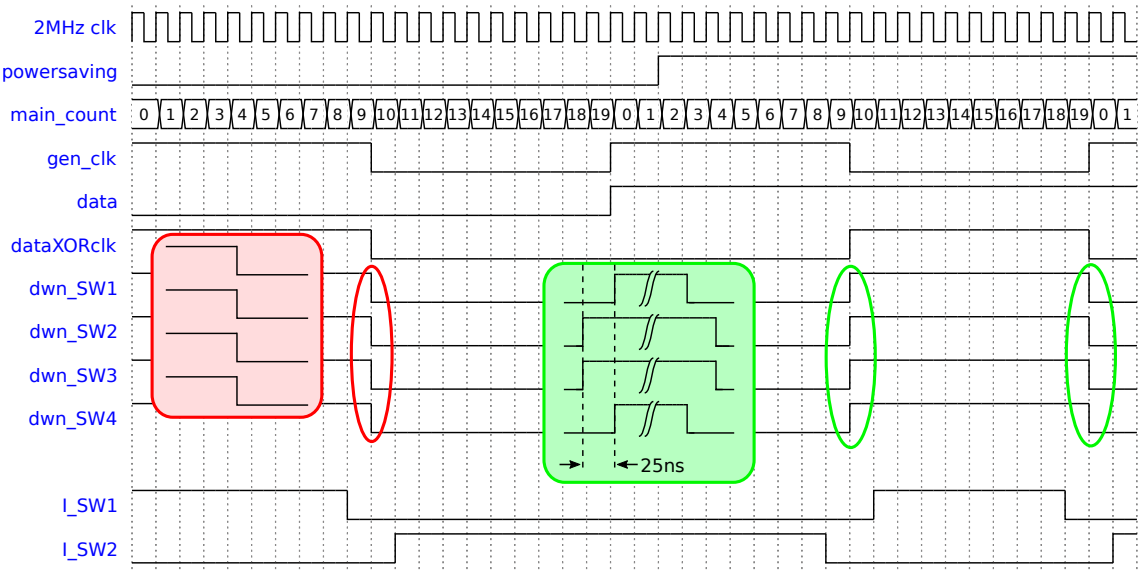


Figure 5.2: Timing diagram of downlink module with power saving low to high.

to the multiplexer responsible for the I_{DOWN} measuring circuit (shown in Figure 5.2 by signals *I_SW1* and *I_SW2*). A dead-time of 1 clock cycle at 2 MHz is also used to ensure that when the NO switch is turned on (through I_SW1/I_SW2), the multiplexed signal is 'ground' and not V_{DOWN}.

5.1.2 The Power Supply Module

In order to update the voltage, V_{DOWN}, the tap points of the digPOTs need to be changed accordingly. To change the tap point of one potentiometer by x amount, x cycles need to be sent on the *INC* line of the digPOT. The direction of change (whether it is up or down the resistor array) is set by the *U/D* line as illustrated in Figure 5.3. However, since three potentiometers are used in series, there are several ways of adding/decreasing the number of taps. For instance, should 24 taps need to be added, one can: (1) add 24 taps to pot 1; (2) add 12 taps each to pot 1 and pot 2; or (3) add 8 taps each to pot 1, pot 2 and pot 3. Thus, to keep the design as flexible as possible to changes, all necessary logic was designed in such a manner that based on the user's choice, the potentiometers can be updated one/two/three at a time. Other logic was also used to ensure that if one (or more) potentiometer's tap count saturates, another digPOT is updated instead.

These design choices required the use of a 5-bit counter for each digPOT to keep

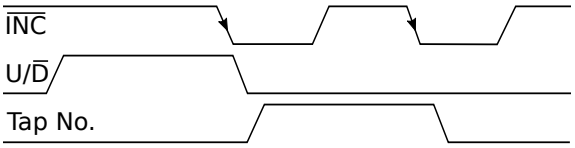
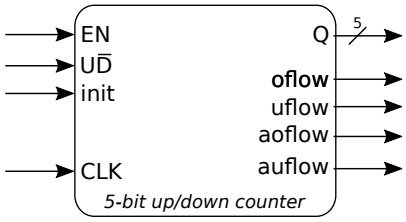
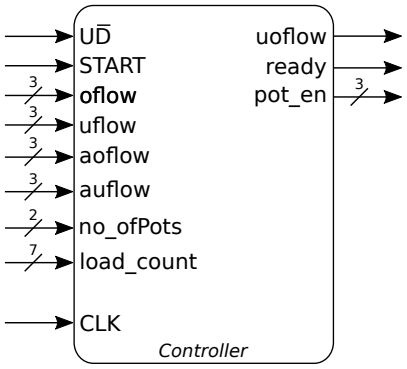


Figure 5.3: Digital potentiometer up/down interface – Tap number is updated on the falling edge of the INC signal.

track of the current tap position of the device. Such counter has also overflow, underflow and almost over/under flow flags to signal the main system that a particular potentiometer has saturated (or will saturate on the next increment/decrement). In Figure 5.4a these are denoted as *oflow*, *uflow*, *aoflow* and *auflow* respectively.



(a) A 5-bit up/down counter used for each potentiometer.



(b) A 7-bit down counter with a variable decrement (1/2/3) – used to track changes in tap position.

Figure 5.4: Counters used to keep track and update the tap positions of the digital potentiometers.

A controller (Figure 5.4b) then detects which potentiometers to update depending on: the flags from the 5-bit counters, the number of tap inc/decrements required (*load_count*) and the maximum number of digPOTs as set by the user (*no_ofPots*). It also utilises a 7-bit down counter, *cntrlr_count*, to keep track of the amount of tap changes left. This counter is decreased by one/two/three on each clock cycle, depending on *no_ofPots*. Once its count reaches zero, the module asserts its *ready* line to signal that the digPOTs have been successfully updated. In the event that all 5-bit counters are saturated, and the count is not zero, *uoflow* is asserted, signalling an error to the system.

Figure 5.5 shows a case where the system decreases the current tap position of the digPOTs by 20. Initially, each potentiometer has its wiper position set to midscale (on power-up) as seen by *count_pot0* and *count_pot1* (having a value of 15). Since the user has

specified no_ofPots to be 1, the system updates just one digPOT at a time. But as one potentiometer has only 32 taps, the uflow flag is asserted after 15 cycles, and the controller switches to another potentiometer.

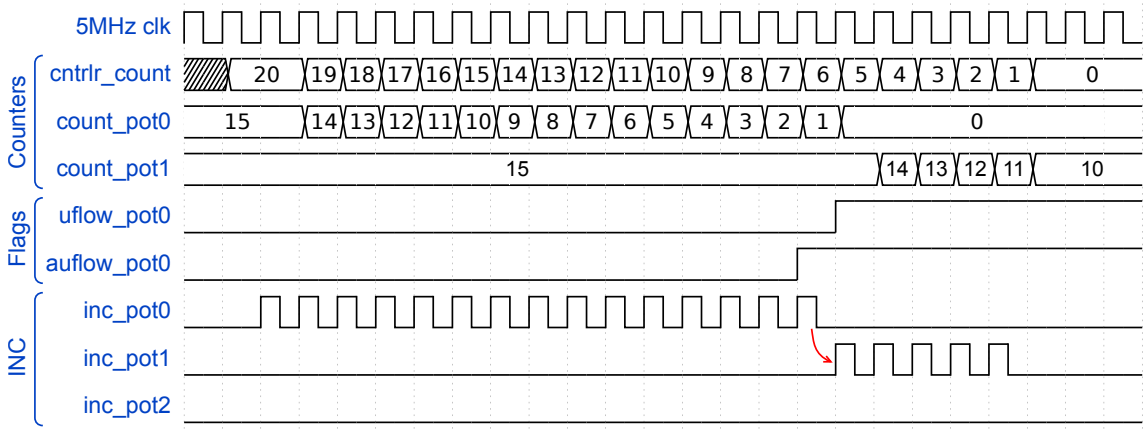


Figure 5.5: Updating digital potentiometers with *no_ofPots*=1, *load_count*=20, and *UD̄*=0. When the *uflow* flag on one device goes high, the controller switches to another device whose *uflow* flag is low.

5.1.3 The Current Feedback Module

In order to measure the current, communication with the ADC is required, as shown in Figure 5.6(a). This is done by a simple interface, compatible with SPI. The ADC needs one/two pulses (depending on which channel is selected) on its *CNVST* pin to start conversion. A delay of approximately 7.5 µs is then required to ensure that both acquisition and conversion processes have taken place. Following this delay, eight clock cycles are then sent to the ADC for data to be received by the FPGA. As a result, if one were to use the interface at its maximum frequency, the minimum time required to obtain a new sample is $9 \times 1/5\,\text{MHz} + 7.5\,\mu\text{s} = 9.3\,\mu\text{s}$; giving a maximum sampling rate of 107.526 kSps. Hence, to synchronize the sample instant with the downlink waveform, a sampling rate of 100 kSps was selected. This sampling rate is used either completely by sampling I_{DOWN}, or if requested by the user, divided into 50 kSps for I_{DOWN} and 50 kSps for V_{DOWN}.

Additionally, to ensure that any glitches on the sampled current do not result in a large change in V_{DOWN}, a moving average is implemented in hardware as depicted in Figure 5.6(b). The length of the moving average depends on the sampling rate of the

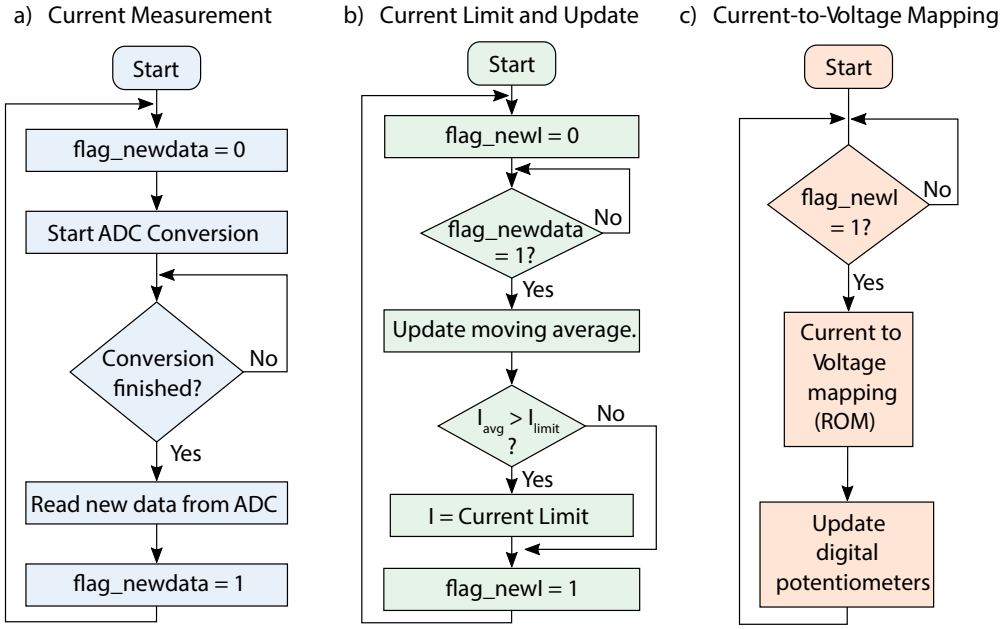


Figure 5.6: Digital control algorithm for evaluation and feedback.

current. Whilst for 100 kSps, the length is eight samples, that for 50 kSps is four samples. These lengths were chosen to ensure that for a step input, the output settles within 100 µs; 10 times faster than the bandwidth of the measured signal (1 kHz mentioned in Section 4.4). To avoid adding all samples each time a new sample is available, the Moving Average (MA) was implemented using Equation 5.1, whereby a scaled version of both the oldest and newest samples are deducted and added respectively.

$$MA_n = MA_{n-1} - \frac{x_{n-m-1}}{m} + \frac{x_n}{m} \tag{5.1}$$

where:

n is the current sample

m is the length of the moving average

x is a sample

Apart from the moving average, a programmable current limit is also available to ensure that the current does not exceed a certain value. This is mostly required when a small number of optrodes are connected to the system (to ensure that V_{DOWN} saturates at a lower voltage), and when a short is developed in the system. After the new sample is received, the moving average updated, and its result checked to ensure that it is less than

the set limit, it is used to obtain a new V_{DOWN} (Figure 5.6(c)). This is done by an internal Read Only Memory (ROM) in the FPGA which stores the relationship between I_{DOWN} and the potentiometer's tap position. The VHDL file for this ROM is automatically generated using a script written in MATLAB. It is based on a number of parameters, namely: R_{cable}, $I_{DOWN,max}$, $V_{rectifier\_drop}$, $V_{@brain}$, maximum number of taps, R1, and R2 (used for the variable power supply). For instance, for different values of R1 and R2 (as found in PCU_v1 and PCU_v2), a different relationship is obtained, starting from different tap positions as depicted in Figure 5.7.

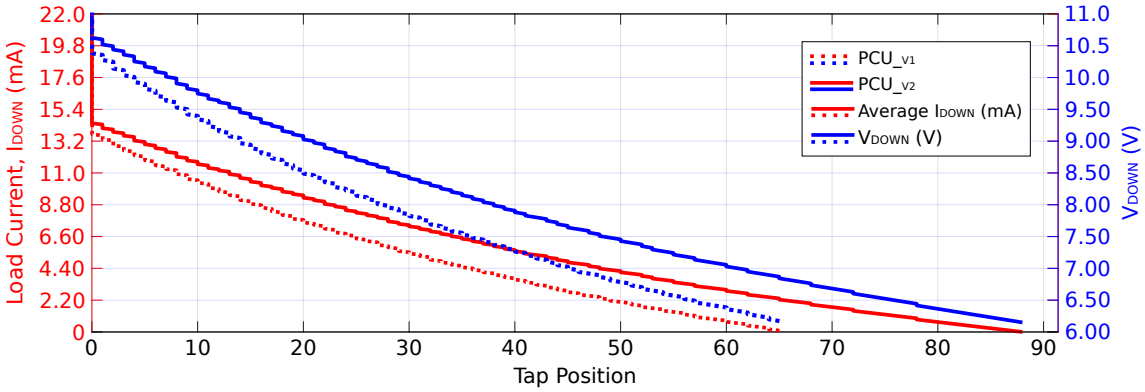


Figure 5.7: A graph of I_{DOWN} and V_{DOWN} against tap position for both PCB prototypes.

The implementation of this module uses a Finite State Machine (FSM) clocked at 40 MHz with five states, as shown in Figure 5.8. Each state functions as follows:

- *reset* – resets the whole system to the power-on state. This is done by resetting all signals and registers to their default state. Additionally, since sub-modules (such as the ADC controller and the power supply modules) use lower clock frequencies, the reset state is held for 50, 40 MHz cycles to ensure that the reset signal has been registered by these modules.
- *initial* – re-initialises the power supply (useful when the user specifies a new power-on voltage). This is achieved by first disabling the power supply. Then all digital potentiometers are saturated to set a point of reference (just in case the counters do not match the actual tap position of the devices) and re-initialised to mid-scale (or to the value requested by the user). The power supply is finally enabled, generating the required voltage.

- *idle* – the system state when downlink is not enabled. When downlink is enabled, the idle state delays the start of the downlink process such that the ADC samples are synchronised with the downlink.
- *Iacquire* – ensures an acquisition and conversion of a new sample for I_{DOWN}. It first disables the ADC module, allowing the previous data to be read. This data may be either a voltage (if the user requires V_{DOWN} values from the GUI) or a current. Should it be the latter, the appropriate registers are updated, and the whole process shown in Figure 5.6 is performed in parallel. The ADC is then enabled for the next sample.
- *Vacquire* – ensures an acquisition and conversion of a new sample for V_{DOWN}. This is similar to the state above. Since however, the input of the ADC is multiplexed, the previous sample for V_{DOWN} will always be I_{DOWN}. Therefore the value of I_{DOWN} is updated and a conversion for V_{DOWN} is initiated.

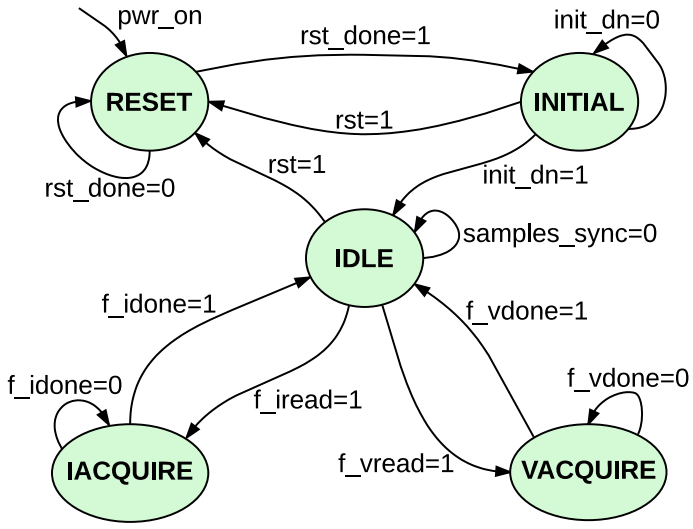


Figure 5.8: Finite state machine diagram for the current feedback module.

5.1.4 The Uplink Module

Due to the complexity of the analogue circuitry for the uplink system, and the considerable amount of variables that may change the system's response, a robust algorithm is required to decode the data received from the optrodes. Thus first, the received uplink signal is guarded against metastability by using a shift register four bits long. The uplink is then

delayed by a certain amount (using shift registers) so that both the uplink and downlink (obtained from another comparator) waveforms are synchronised. Finally, the signal is de-bounced to remove any short pulses.

The signal is then fed to the algorithm used to decode the data. The general idea behind this algorithm is that of using a gated counter. Such counter has a clock source and an enable pin which is used to gate the clock signal. Whilst in single level mode, the counter is used to measure a pulse width of a specific polarity (1 or 0), in toggle mode, the counter is made to measure the pulse width of both polarities (1 and 0). The latter is used in the above-mentioned algorithm as both polarities are important. Additionally, since the interface makes use of phase encoding, there are two different pulse widths that can appear in the signal, as depicted in Figure 5.9.

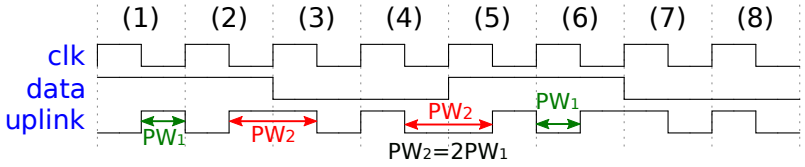


Figure 5.9: Phase encoding results in two different pulse widths.

The following is the sequence implemented using a finite state machine in which data is decoded from the uplink:

1. For the decoding to start, the algorithm waits for the synchronisation bits (a 1 followed by a 0 in data – (2) and (3) in Figure 5.9) during the *idle* state. These bits result in a sequence of short_0-long_1-short_0 when they are phase encoded. Thus, the algorithm waits for a short low period, followed by a long high period. This feature is important as it ensures that whatever the polarity of the uplink signal during idle periods, the data packets are still decoded successfully.
2. Once such periods are detected, these are checked in the *checking* state to ensure that they are within the set thresholds which depend on the current data rate.
3. If the periods are too short or too long, the algorithm returns to the *idle* state. Else, the system progresses to the *counting* state.
4. In the *counting* state, the pulse widths obtained from the counter are compared against specific thresholds to identify the length of the pulse.

5. In the case where the pulse is long, two identical bits (of the same polarity as the uplink signal) are shifted into a shift register. On the other hand, should the pulse be a short one, only one bit is shifted in the register. This mechanism is applied to both low and high periods and it is repeated for all bits.
6. Once 24 bits (total number of bits in one packet, excluding synchronisation bits) are received, a total of 48 bits should be in the shift register, since 1 bit has both a low and a high period.
7. In the case where the data has been decoded correctly, when the contents of the shift register are XOR'ed with an alternating stream of 1s and 0s, the resulting packet should have each data bit repeated twice (for example, if the encoded data was 1011_2, the resulting packet after XOR'ing should be 11001111_2).
8. If this is not the case, then the data is wrong. However if the opposite happens, there may still be the possibility that two errors cancel out each other, and the data appears to be right. Thus, the data needs to be validated. For this project, no other error correction methods were investigated (apart from the self-checking method of phase encoding).

It is also important to note that during the *counting* state, through the use of the downlink input, downlink glitches present on the uplink wires are compensated for. This is done by increasing the pulse width by one/two clock cycles for the period that is affected; hence, ensuring that the pulse width is classified correctly.

5.1.5 The Main Controller Module

As the name implies, this module is mainly responsible for controlling and monitoring the system to ensure correct operation. Additionally, it is in charge of the interface between the GUI and the FPGA board (Universal Asynchronous Receiver/Transmitter (UART)). Such an interface uses a simple state machine comprising of three states, namely:

- *idle* – no operation is executed. This state is run when no activity is present on the UART interface.
- *cmd* - this state is used for commands. Upon receiving the first byte (being the

command), it is decoded, and the number of bytes (of data) to be received following this command byte is stored. The commands that are currently available for this system are listed in Table 5.1.

- *data* - in this state, the bytes received are decoded, and any system flags are set here. Since there are several commands which require more than one data byte, the *data* state is repeatedly executed until the number of data bytes received matches that programmed for.

It is important to note that the baud rate used for the UART is 128 kbps as this is the maximum rate supported by the personal computer (PC) used. Since the sampling rate of the ADC is 100 kSps, it is not possible to send all samples to the GUI as this would require a baud rate of at least 800 kbps (each sample is 8 bits long). Therefore, the samples obtained from the ADC are sub-sampled by a factor of 30 to ensure that the data rate (now less than 50 kbps) does not exceed the baud rate (128 kbps). This is enough to allow a synchronisation byte to be put with each sample of I_{DOWN}, so as to differentiate between I_{DOWN} and V_{DOWN} samples when both are sent to the GUI.

5.2 User Interface

As one would expect, such a system requires several inputs to run, such as the downlink enable and the 24-bit (downlink) data packet. One way of inputting this data whilst the system is running is by using push-buttons and switches. This approach however, is limited by the number of buttons and switches. It also becomes impractical as system complexity increases. Thus, this author opted for the development of a GUI which can communicate with the system via the available UART port connected to the FPGA. This completely hides the physical interface used to update the system from the user. Notwithstanding this, it is more important that the GUI is fast and easy to use.

The first decision faced by the author was that of what programming language to be used in developing this piece of software. Two packages were identified as good candidates, namely:

1. LabVIEW – a graphical programming language which represents the flow of data

Table 5.1: UART instructions format and description

Instruction	*First byte sent*	*Other bytes sent*	*System default*	*Comments*	*Bytes received from FPGA*
System monitoring					
System reset	$0xFF_{16}$	–	0_{10}	–	–
Get I_{DOWN} and/or V_{DOWN} readings and use DIP or I_{DOWN} for current to tap count mapping	$0x10_{16}$	X00X 000X	$1000\,0000_2$	MSB_1 - DIP SWs enabled Bit 4_1 - Enable V_{DOWN} Bit 0_1 - Enable I_{DOWN}	*Current and/or voltage readings
Downlink Output					
Output $enable_1$/$disable_0$	$0x01_{16}$	$0000\,000X_2$	0_{10}	–	–
Update data register	$0x40_{16}$	$0xXX_{16}\times3$	$0_{10}\times3$	24-bit data. LSB sent first	–
Update data register and loop	$0x41_{16}$	$0xXX_{16}\times3$	$0_{10}\times3$	24-bit data. LSB sent first	–
$Enable_1$/$disable_0$ dynamic power dissipation reduction	$0x42_{16}$	$0000\,000X_2$	0_{10}	–	–
Downlink Supply					
Send power-on potentiometer tap position	$0x02_{16}$	$0XXX\,XXXX_2$	$0010\,1101_2$	–	–
Set number of potentiometers that can be updated at once	$0x03_{16}$	$0000\,00XX_2$	$0000\,0011_2$	–	–
Current Feedback System					
$Enable_1$/$disable_0$ load current switches	$0x20_{16}$	$000X\,000X_2$	0_{10}	Bit 0 - SW1, Bit 1 - SW2	–
Set I_{DOWN} current limit	$0x21_{16}$	$XXXX\,XXXX_2$	$0011\,1001_2$	–	–
Uplink					
Input $enable_1$ and $reset_1$	$0x80_{16}$	$X000\,000X_2$	0_{10}	LSB_1 - input enabled MSB_1 - uplink reset	–
$Send_1$ data received to GUI	$0x81_{16}$	$0000\,000X_2$	0_{10}	–	Uplink data
Change data rate	$0x82_{16}$	$0000\,0XXX_2$	0_{10}	0 - 1.6 Mbps; 1 - 800 kbps	–
$Reset_1$ BER counter and/or $send_1$ count to GUI	$0x83_{16}$	$X000\,000X_2$	0_{10}	LSB_1 - reset counter MSB_1 - send count	BER count

*When both I_{DOWN} and V_{DOWN} values are received, a synchronisation byte of $0101\,0101_2$ is put just before the value for I_{DOWN}.

throughout the execution of the program. However, several known constructs such as loops and sequences, are also available.

2. MATLAB – mostly used for data manipulation. It has now evolved to include communication with external devices and also GUI development.

Table 5.2, was used to compare between the two software packages, and select the right one. In fact, it was concluded that LabVIEW is the right choice due to its ease of implementation when compared to MATLAB.

Table 5.2: GUI programming language selection table [27].

Metric	LabVIEW	MATLAB
Ease of implementation	Being a graphical programming language, it is very easy to build the GUI as it is simply drag and drop. Developing the algorithm to respond to the GUI is not difficult as well.	It offers the GUI Development Environment in which ready made components, such as pushbuttons and sliders are already available. Coding is however required to define what happens when a change has occurred in the GUI.
External interface compatibility	Compatible – using NI VISA serial block	Compatible – using Instrument Control Toolbox
Debugging availability	Available – and any errors detected whilst programming the system are highlighted.	Available – breakpoints.

5.2.1 General Program Structure

The GUI developed in LabVIEW is shown in Figure 5.10. It is divided into sections in order to make it easier to find the required function. The first three rows incorporate several features related to the downlink driver and V_{DOWN}. The fourth row provides for the monitoring of the system by showing the values of I_{DOWN} and V_{DOWN}. Last but not least, the bottom row has several features that are used for the uplink part of the interface.

Unless any data is being received from the FPGA, whilst idle, no operations are necessary by the GUI. Hence, the algorithm implemented in LabVIEW is designed to be mainly event-driven by user input. This has been programmed by using an *Event Structure* which waits until a specific event occurs, and then executes the appropriate case to handle such event. Multiple cases are available for each input, each sending the required command and data bytes via UART to the FPGA. For instance, the case for the

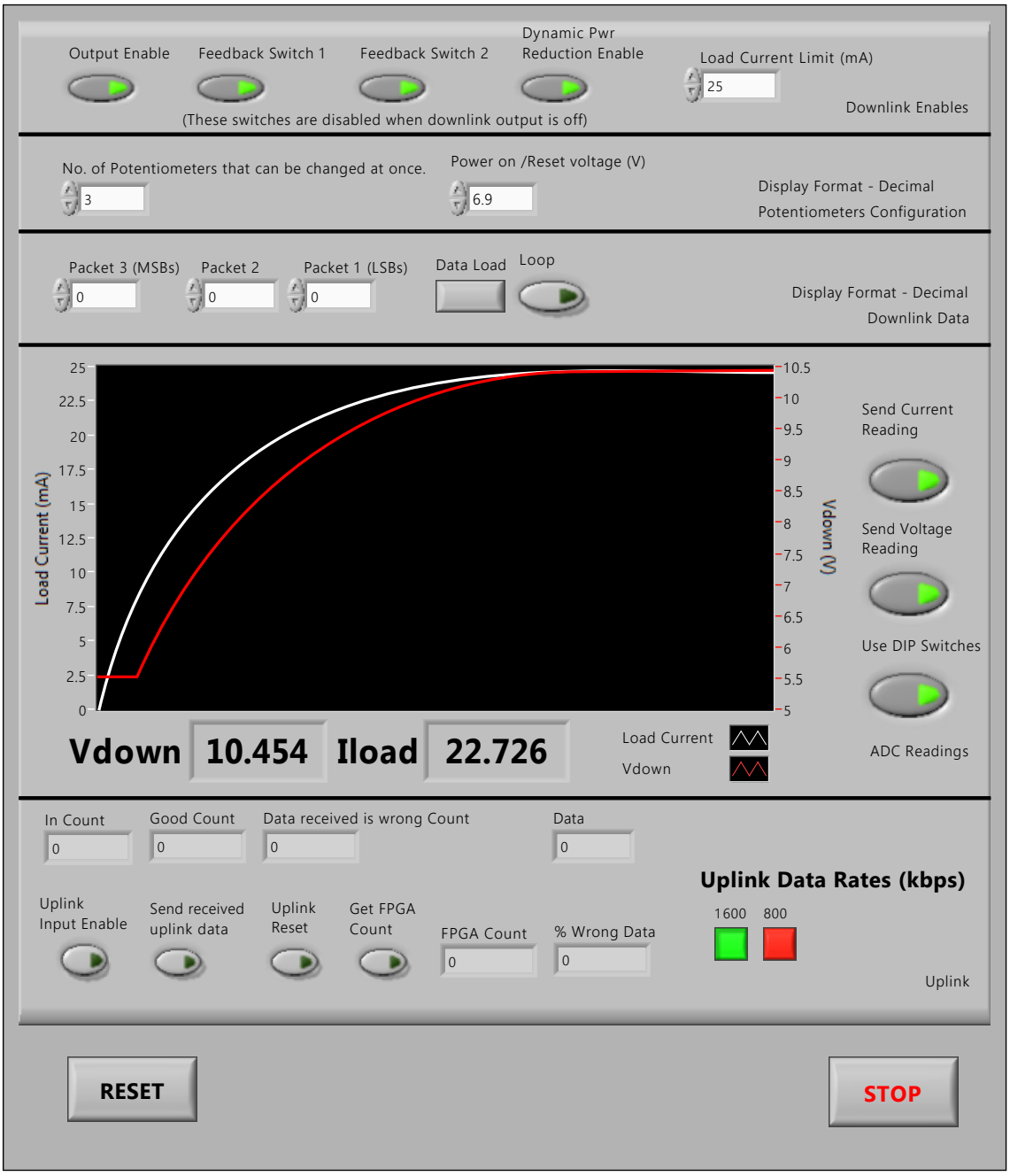


Figure 5.10: The GUI developed using LabVIEW.

downlink output enable is illustrated in Figure 5.11. When no change is detected in any of the inputs within 2 ms, a *Timeout* case is executed. By using this case, it is possible to receive data from the FPGA. However, only one set of data can be received. For instance, the algorithm cannot receive uplink data and ADC samples concurrently (as this would have made the implementation in the FPGA more complex). Therefore data is prioritised as follows (with 1 having highest priority):

1. ADC readings (V_{DOWN} and I_{DOWN} both have the same priority).
2. Uplink data received from the brain implants.
3. Uplink BER count.

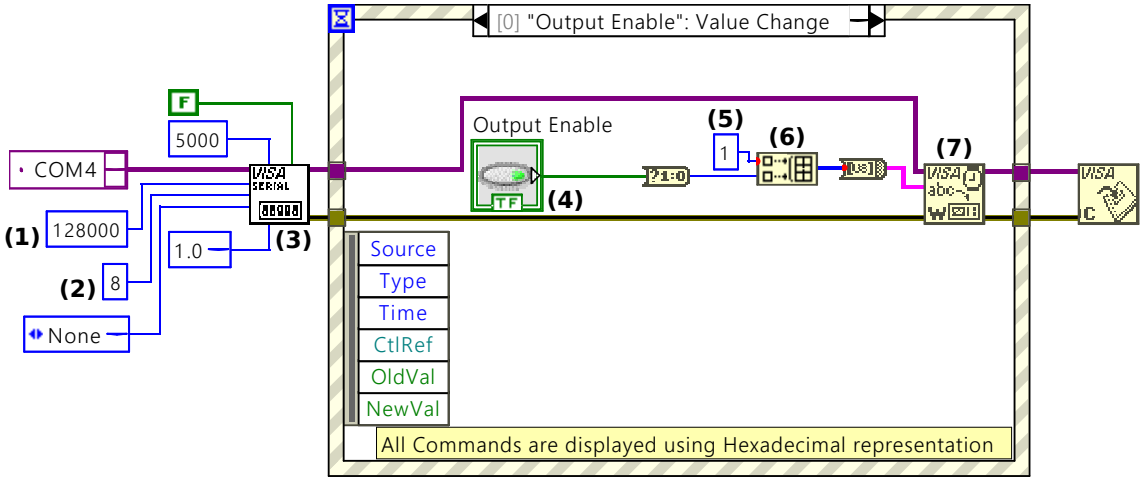


Figure 5.11: The case in the event structure for *downlink output enable* input switch; (1) baud rate; (2) number of bits; (3) configure serial port block; (4) *Output enable* flag input; (5) corresponding command in hexadecimal; (6) build array; (7) write string data to serial port.

5.2.2 System Monitoring

For continuous monitoring of I_{DOWN} and V_{DOWN}, the GUI incorporates a waveform view, to better visualise transients on both signals. It also includes a simple readout so as to obtain a more accurate reading of the instantaneous values. It is also possible to save the received values in a *.csv* file for external use. This option is however, disabled by default to ensure that no large data files are created without the user's approval.

5.2.3 Downlink

Apart from the basic features, such as enabling the output of the downlink driver and dynamic power reduction enable, the GUI provides additional features, such as changing the number of digPOTs that can be updated at once and setting the power-on voltage of the power supply. Last but not least, data can be sent to the FPGA, which is then directed to the brain implants through the downlink driver. This data can also be looped, and therefore sent continuously to the brain implants without user intervention.

5.2.4 Uplink

Similar to the downlink, the uplink has also an input enable, and a module reset. Additionally, to obtain a measure of the BER, any data received through the uplink needs to be verified to ensure that it is correct. Hence, another feature relates to the capability of sending data received from the brain implants to the GUI. Last but not least, the data rate for the uplink can be changed; thereby updating both the tunable low pass filter on PCU_v2 and the pulse width thresholds in the FPGA.

5.3 Summary

Similar to the previous chapter, this chapter contains a description of the design process for the firmware required by the system. The FPGA system is divided into smaller modules namely, downlink, power supply, current feedback, uplink, and last but not least the main controller. All module's implementations are described and a summary of their features is illustrated in Table 5.3. The last module, the main controller is responsible of: monitoring the system by setting the appropriate flags and communicating with the GUI through a UART connection. The list of commands sent through the GUI accepted by the system are also provided. Finally the architecture used for the GUI is detailed, comprising mainly of an event structure. When a specific event occurs (indicated by the structure's properties), the appropriate sequence of commands are executed. Hence, the developed GUI is mainly event driven.

Table 5.3: Software Design - summary table

Module/Feature	*Specification*
Downlink Module	
Deadtime	1 clock cycle (25 ns)
Power Supply Module	
No. of digPOTs that can be update at once	1/2/3
Current feedback module	
I_{DOWN} sampling rate	100 kSps/50 kSps
V_{DOWN} sampling rate	50 kSps
Synchronised with downlink?	Yes
Moving average length	8/4 samples
Current to voltage mapping - storage	ROM - created using a MATLAB script
Uplink Module	
Tunable LPF	800 kHz/1.6 MHz
System stability	Guarding against metastability and debouncing.
Algorithm error detection	Yes, basic - manchester encoding
Algorithm error correction	No
Main Controller Module	
UART baud rate	128 kbps
Bi-direction communication?	Yes, sends uplink data/Uplink BER counter/I_{DOWN} and/or V_{DOWN} readings.

Chapter 6

Testing, Results and Discussion

AS with any system design, testing is a fundamental process required to ensure proper and correct operation of the system. It is important to test the system at each stage of development to ensure that errors/problems do not accumulate and to confirm that each stage has been implemented up to the set specifications.

The following constitutes the sequence of testing performed at each stage, as identified in Figure 6.1:

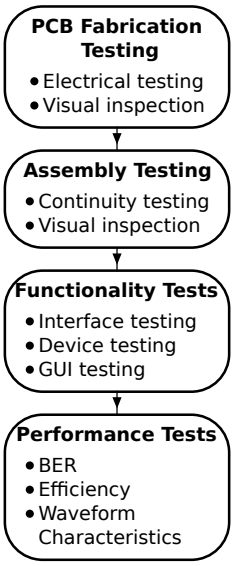
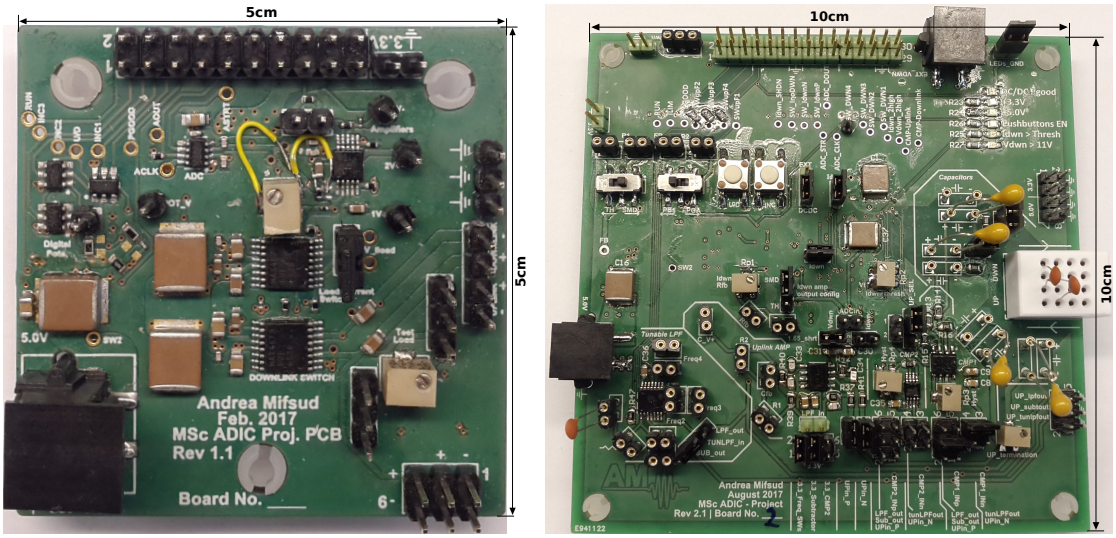


Figure 6.1: System testing sequence

1. **PCB Manufacturing Testing** – Subsequent to the fabrication of the PCB, the boards are visually checked and also electrically tested to ensure that no undesired shorts/opens are present.
2. **Assembly Testing** – During the soldering process, the board is continuously checked to ensure that the components are soldered properly without creating any shorts.
3. **Functionality Testing** – Once assembled, the main components of the PCB are tested to ensure that they are operating according to design.
4. **Performance Testing** – Finally the system is tested at its maximum performance to obtain it characteristics.

This thesis will cover the last two processes of testing, namely functionality and perfor-

mance testing which are performed after the PCB is assembled. The assembled PCBs are exhibited in Figure 6.2. Both prototypes have been tested. However, only results obtained from PCU_v2 will be shown, as this presents a better solution than PCU_v1.



(a) Assembled PCU_v1 **(b) Assembled PCU_v2**

Figure 6.2: Assembled PCBs

6.1 Functionality Testing

Each subsystem is tested to ensure correct functionality. By simply powering on the PCB, the digital potentiometers should have their wiper set to midscale. As a result, if enabled, the output voltage of the DC/DC converter should be equal to the result from Equation 6.1.

$$V_{out} = \frac{R1 + R2 + 300\,k\Omega}{R2 + 300\,k\Omega} = 6.9\,V_{PCU\_v1}/7.57\,V_{PCU\_v2} \tag{6.1}$$

Following power up, the communication interfaces are checked, ensuring that the device/subsystem is responding as expected. For instance, normal operation of the SPI compatible interface of the ADC is shown in Figure 6.3. The GUI is also tested; whereby a specific input is changed, and if communication is set up correctly, the expected change is observed in the system.

On the other hand, for the downlink driver and uplink receiver, a function generator

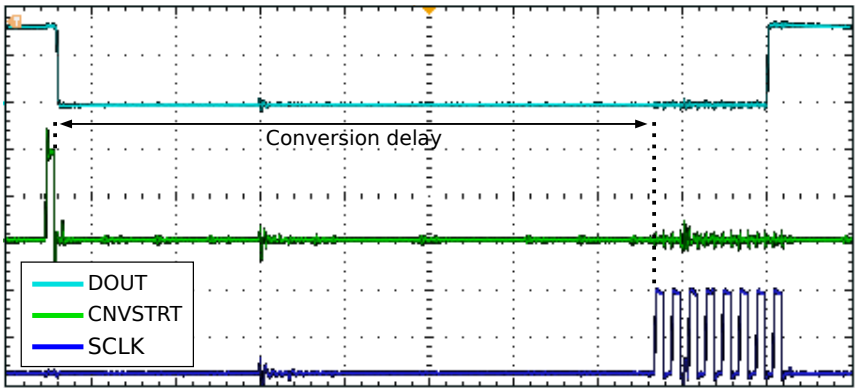


Figure 6.3: Functionality testing – SPI compatible ADC interface.

is required to set the appropriate waveforms at their inputs. For the downlink driver, a square wave at 100 kHz was used, and its output, a similar square wave with its amplitude equal to V_{DOWN} was observed. With regards to the uplink, a square wave with a small amplitude (≈mV) at 1.6 MHz was used as an input, and the output monitored to ensure that a CMOS 3.3 V compatible signal was obtained.

6.2 Performance Testing

After confirming that each subsystem was operating according to its design, performance testing was executed to obtain the characteristics of the designed system. This section will therefore, first highlight the equipment and test setups used, and then the results are presented and discussed.

6.2.1 Equipment Used and Test Setup

A list of the equipment used to carry out the following tests can be found below:

- Oscilloscope – LeCroy 434 - 350 MHz Oscilloscope 2 GS/s
  - Active differential probe, AP034. All signals at the 4-Wire interface Integrated Circuit (4WIC) PCB were measured differentially using this probe.
  - 3 passive probes, TEK P6139A.
- Oscilloscope and Logic Analyser – MSO2014 Mixed Signal Oscilloscope 1 GS/s
- Function Generator – AFG3102 Dual Channel Arbitrary Function Generator. This was used for the uplink communication in order to send data and enable signals via

an isolator to the 4WIC PCB.

- Power Supply - 2 × digimess DC Power Supply HY3003 and 2281S-20-6 Precision DC Supply – one power supply was used in isolated mode (ground not shorted to the earth terminal) to power the uplink isolator. The other two were used to power on the PCU, with 3.3 V and 5 V.

Apart from the equipment utilised, it is also important to note the test setups used for these tests. For the downlink tests required to calculate efficiency, waveform characteristics and loop settling time, Figure 6.4 is applied as a test setup. On the *brain* side of the interface, the downlink is connected across a variable dummy resistive load that is varied according to the load current required. Additionally, a current measuring resistor of 50 Ω is used to measure the average current flowing through the load. On the other hand, for the downlink and uplink readings related to BER, Figure 6.5 is applied as the experimental setup. This setting enabled this author to test the implemented PCUs with the 4WIC developed at Imperial College London; hence obtaining accurate and realistic results.

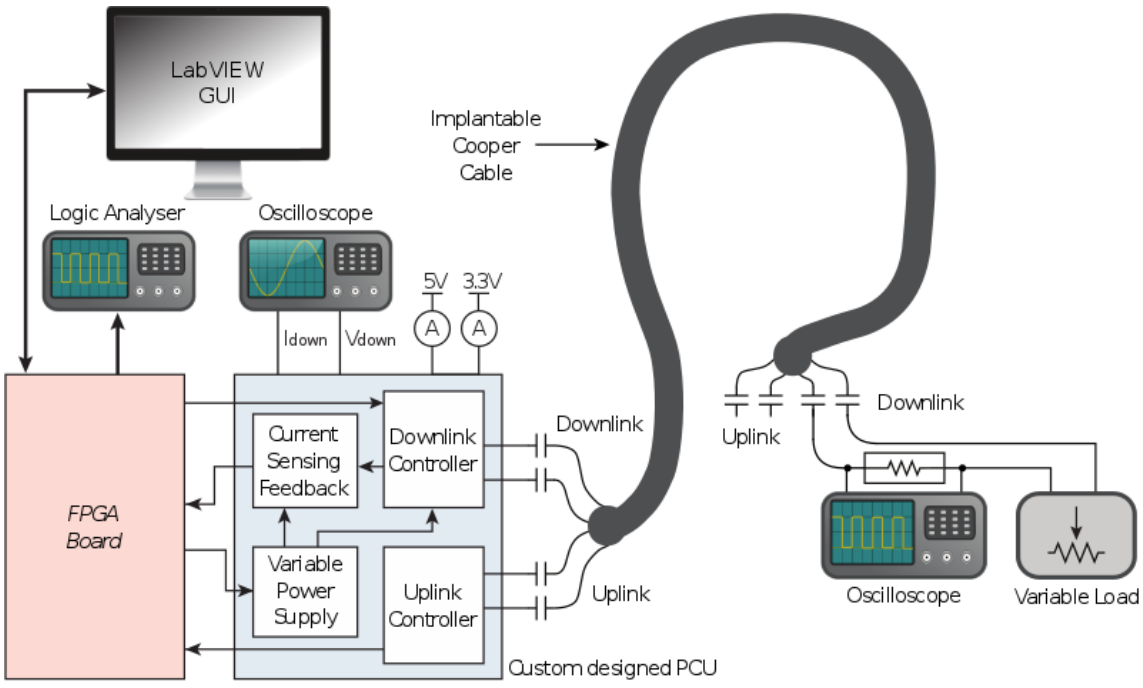


Figure 6.4: Test setup 1 - using a dummy resistive load.

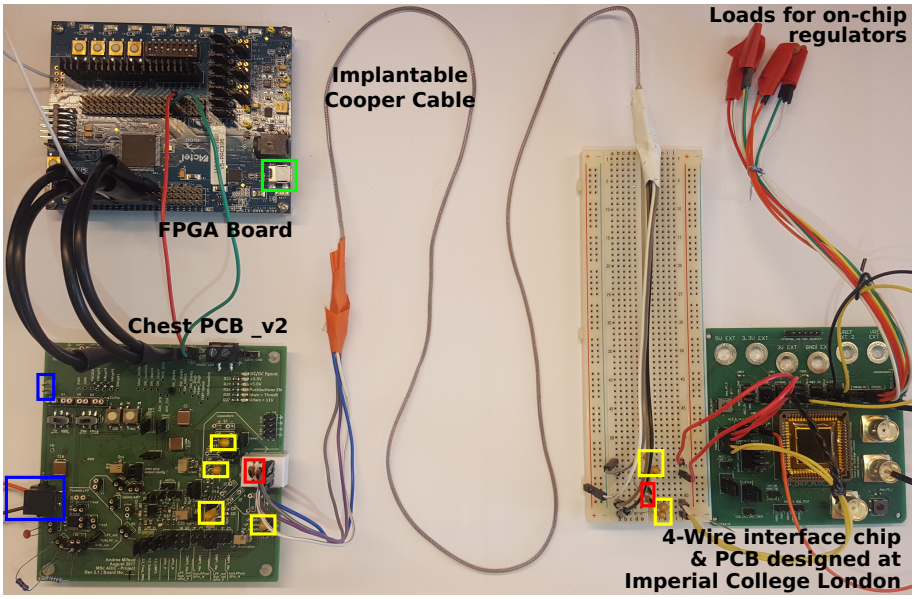


Figure 6.5: Test setup 2 - using 1 4WIC PCB; ■ Power input; ■ AC coupling capacitors; ■ Capacitance equalisation network; ■ Power and UART communication.

6.2.2 Downlink Testing and Results

The chest unit has to power the brain implant through the downlink connection, using an AC-coupled pair of wires. This is done using a differential configuration, with the square wave being the waveform of choice. The frequency used is 100 kHz which is defined from the bit rate (100 kbps) as apart from power, data communication with the implant is also required. So, what follows are the tests and results obtained; characterising both the power delivery and the data communication aspects of this interface.

6.2.2.1 Waveform Characteristics

It is vital that the waveform sent through the Cooper cable is as smooth as possible, since any glitches on this waveform may appear on the rectified output of the optrode, possibly affecting core systems in the chip. Figure 6.6 shows the voltage at the output of the optrode ($\approx$5 V) with the corresponding waveform at the input of the cable. The Figure reveals that even though there are some oscillations in the downlink waveform, these are not visible on the rectifier's output. This may be due to the reservoir capacitor at the output of the rectifier which is smoothing the received voltage, and filtering out the oscillations. It may also be due to the passive network formed by the implantable cable. Since this provides

a similar response to a low pass filter, it may be dampening the oscillations received on the other end of the cable. It may also be the case that these oscillations are partly due to the measuring setup, and the probes used during the experiment.

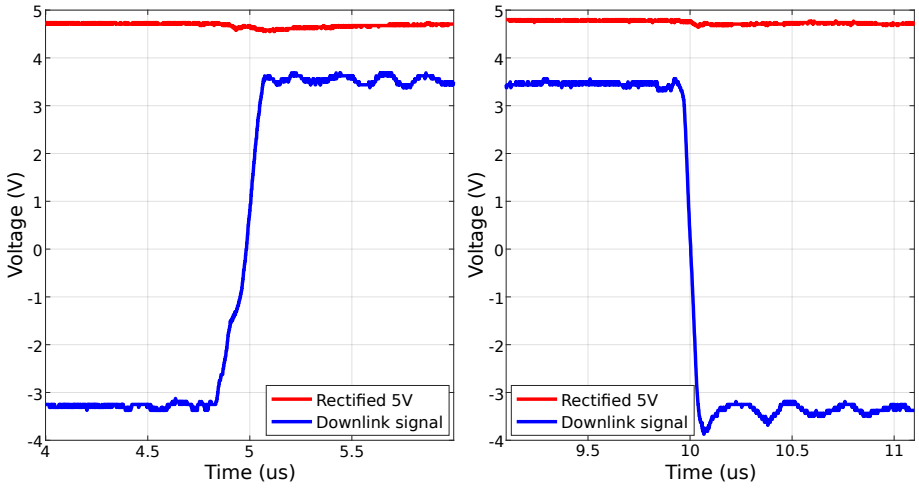


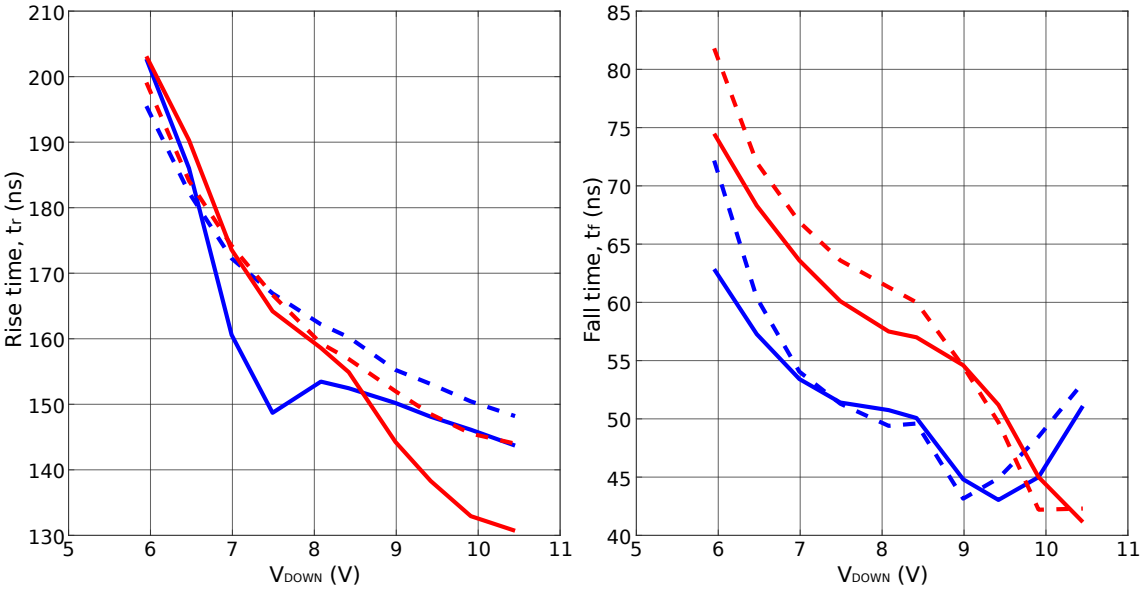
Figure 6.6: Downlink waveform and recovered 5 V at rectifier's output.

Another noteworthy result is the asymmetrical transition times, where the fall time is shorter than the rise time. This is further investigated in the plots depicted in Figure 6.7. This may be attributed to wrong sizes (or ratio of W_P/L_P to W_N/L_N) for PMOS and NMOS switches inside the chip (which result in different drive due to different electron and hole mobility). It may also be due to switch dead-time, whereby the longer the delay, t_d, the higher the transition time, as evinced in Figure 6.7a.

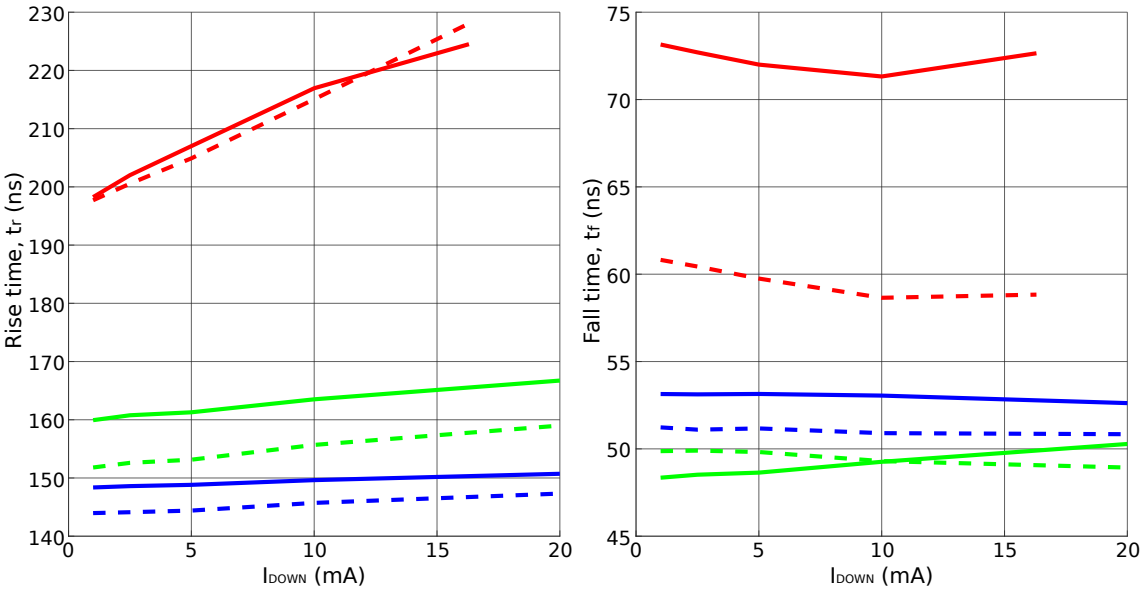
Another variable affecting t_r and t_f considerably is V_{DOWN} as evident in Figure 6.7a. As V_{DOWN} increases, the on-state resistance of the switches decreases (as noticed in Figure 4.6). Hence, more current flows during transitions, charging up any parasitic capacitance at their output node at a faster rate, and therefore decreasing transition times.

6.2.2.2 System Efficiency

Keeping in mind that the CANDO system will be powered using a rechargeable battery, obtaining a highly efficient power delivery architecture is paramount. This minimizes losses and reduces current drawn from the battery, thereby increasing battery life. It may also decrease the system's rise in temperature, mostly due to heat losses – depending on the instantaneous amount of current flowing. The calculated and plotted data seen



(a) A plot of transition time against V_{DOWN} for a load current of 1 mA; ■ with switch dead-time; ■ without switch dead-time; ━ DWN_P; ╍ DWN_N.



(b) A plot of transition time against I_{DOWN} for various V_{DOWN} voltages without switch dead-time; ■ V_{DOWN}=6 V; ■ V_{DOWN}=8.24 V; ■ V_{DOWN}=10.44 V; ━ DWN_P; ╍ DWN_N

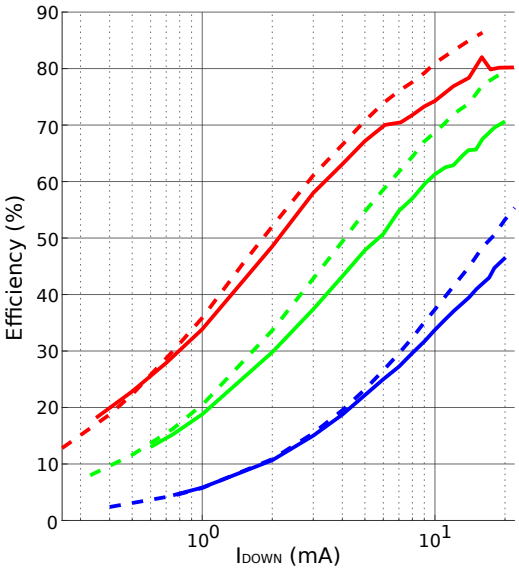
Figure 6.7: Investigating the relationship of waveform transition times (10 % to 90 % of steady state value) against I_{DOWN}, V_{DOWN} and switch dead-time length.

in Figure 6.8a suggests that the efficiency for PCU_v2 is higher than that obtained for PCU_v1. This was expected since PCU_v1 was optimised so as to obtain a higher efficiency in PCU_v2. It is however, important to note that the static power dissipation (when the output of the downlink driver is disabled) of the system has increased in PCU_v2. This may be associated with the reduction (by half) of the reservoir capacitance connected to the output of the driver. As a consequence, when the DC/DC converter is in sleep mode, the drop in V_{DOWN} is twice bigger (since $V = IT/C$). This implies that the DC/DC converter will wake up sooner, and therefore the average input current (required for the output load and to power on the control circuitry of the power supply) will increase. This is also why at low currents PCU_v1 has a higher efficiency than PCU_v2. Apart from normal operation, where all switches are fed the same signal at their input, PCU_v2 has the functionality of sending different signals, hence possibly incorporating dead-time. As expected this feature increases efficiency, especially for high values of V_{DOWN}, as illustrated in Figure 6.8b.

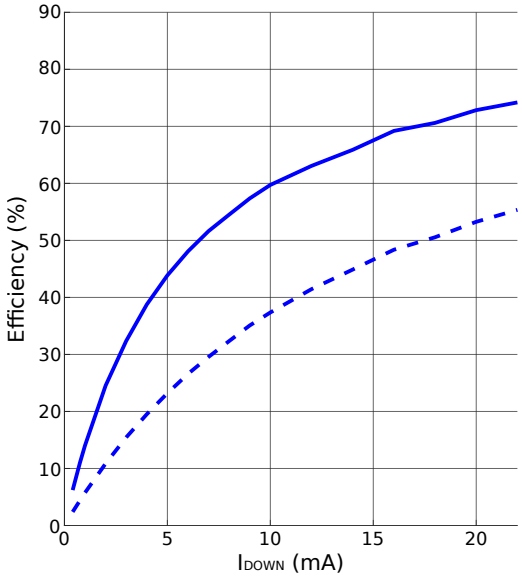
Besides the reduction in the dynamic power dissipation of the switches during output transitions, increasing the dead-time also affects the waveform of the current flowing to the brain implant, as marked in Figure 6.9. The figure reveals that when a dead-time period of 25 ns is used, the current flowing through the cable peaks at a lower value than when compared to the instance when no dead-time is used. As a result, the IR losses in the cable are less, resulting in a higher efficiency.

6.2.2.3 Current Loop Settling Time

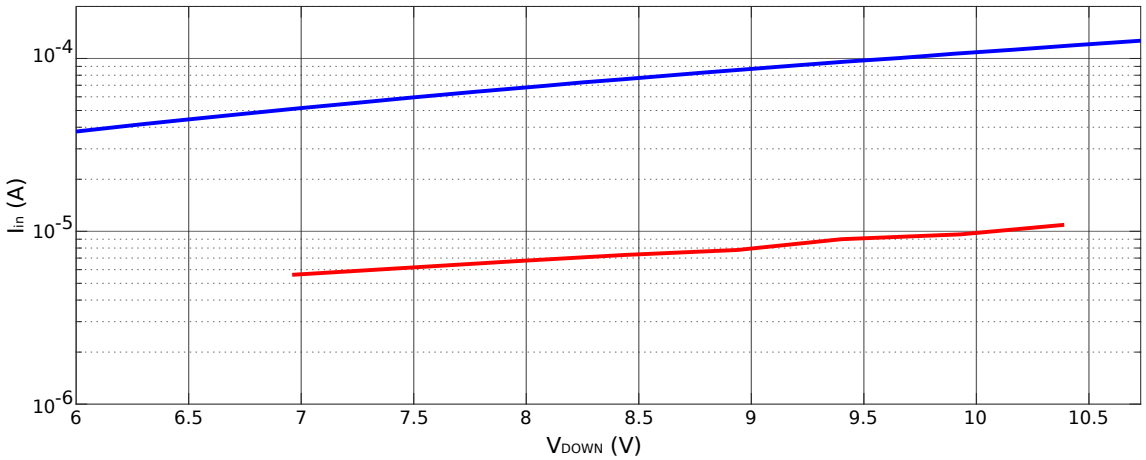
Another two important characteristics of the system are the settling time and stability of the current loop. This is mostly because the load presented by one optrode is that of a μLED switching on/off with a step current between 1–2.3 mA. Thus, a test was developed whereby the maximum, worst case settling time is measured whilst ensuring a stable output. A current sensing resistor was utilised between the AC-coupling capacitor and the implantable cable. On the other side, the implantable cable was connected across a dummy resistive load with a push button in series. The resistance was chosen such that the resulting current was that of 22 mA when V_{DOWN} is equal to approximately 10.4 V.



(a) Downlink power delivery efficiency against I_{DOWN} for 3 different values of V_{DOWN} without switch dead-time; V_{DOWN}=6 V; V_{DOWN}=8.24 V; V_{DOWN}=10.44 V; PCU_v1; PCU_v2.



(b) The effect of dead-time on downlink power delivery efficiency for PCU_v2; with 25 ns dead-time ; without dead-time.



(c) Static current input for both PCU_v1 and PCU_v2 with the downlink driver disabled; PCU_v2; PCU_v1.

Figure 6.8: System efficiency (FPGA board not included) against I_{DOWN} and static power dissipation (with the downlink output driver disabled) for both PCU_v1 and PCU_v2.

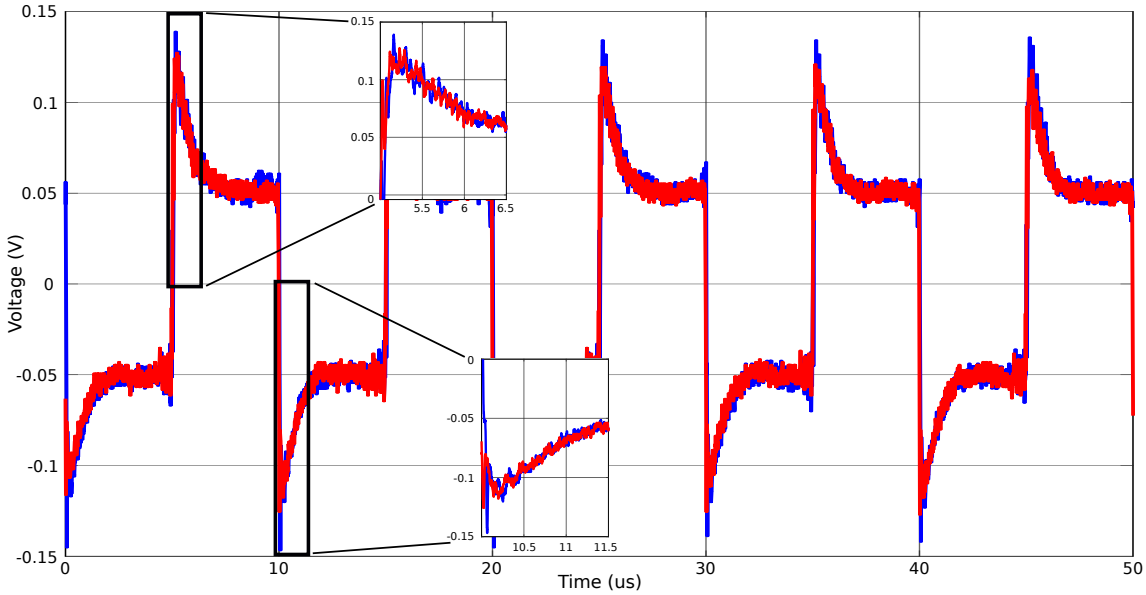


Figure 6.9: A plot of the voltage across a downlink, current sensing, 50 Ω resistor against time; ■ without dead-time; ■ with a 25 ns dead-time. The measured current is the one flowing through the implantable cable and therefore the brain implant. Average load current is 1 mA (0.05 V/50 Ω).

The obtained result is shown in Figure 6.10. Initially, the current settles at approximately 13 mA, increasing linearly as V_{DOWN} increases to compensate for the voltage drop on the cable, until the current measurement saturates at 20 mA. The measured worst case settling time of the system is 1.5 ms. Provided that this is the worst case scenario it constitutes a good result considering that the current signal has a bandwidth of 1 kHz. In the case where the settling time is too high, the ADC needs to be replaced with a higher sampling rate device as it is being used at its maximum sampling rate. Additionally, the length of the moving average can be changed to reduce the settling time of the digital filter itself. Both possibilities need to be further explored.

6.2.2.4 Power Transmission Efficiency

Apart from maximising system efficiency, the Power Transmission Efficiency (PTE) also needs to be maximised to ensure that most of the power available at the chest implant is delivered to the brain implant with minimal losses. This experiment was carried out with the 4WIC connected to the other end of the cable. Additionally, a variable resistor was connected to the rectifier's output to vary the load current; hence varying I_{DOWN}. To

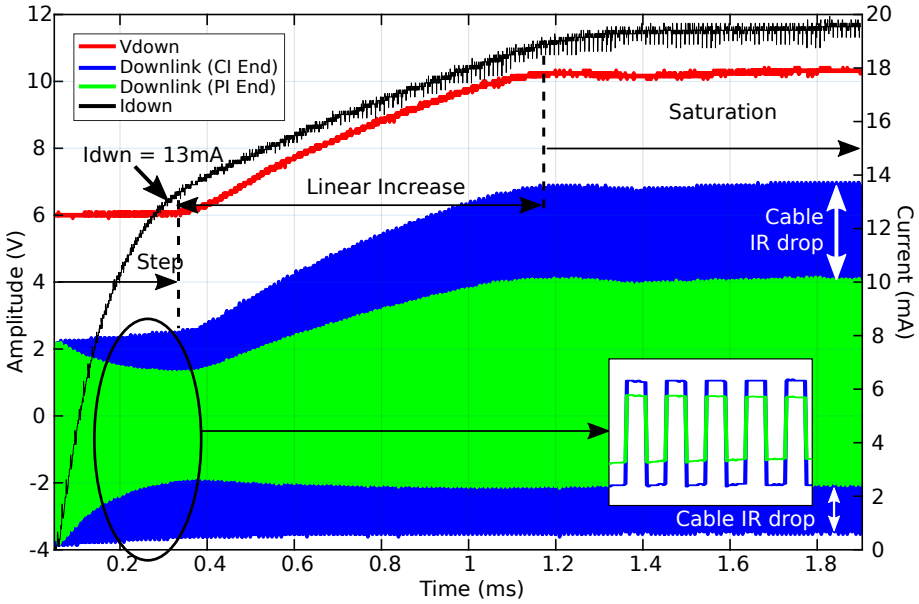


Figure 6.10: System step response using PCU_v1; I_{DOWN}=22 mA at V_{DOWN} = 10.4 V; R_L = 470 Ω.

carry out the necessary calculations for the PTE, the following are required:

1. Calculating the power dissipated by the brain implant (considering the rectifier voltage drop as a loss);
    - The voltage at the output of the optrode's rectifier, V_{rect} – this was obtained by using a multimeter set in voltage mode.
    - The current, I_{brain}, flowing through the rectifier and into the variable resistor connected to its output – this was obtained by utilising a multimeter set as an ammeter.
2. Calculating the power sent by the PCU (without considering any losses in the chest unit);
    - The current, I_{cable}, flowing through the Cooper cable – this was derived by using a current sensing resistor of 100 Ω after the AC coupling capacitors (and before the implantable cable). The voltage drop across the resistor was then measured using a differential probe and scaled accordingly.
    - The differential voltage across the two-wire Cooper cable, V_{D1} and V_{D2} – this was obtained by connecting two single-ended passive probes at those nodes.

Once the waveforms were obtained from the oscilloscope, and the values from the

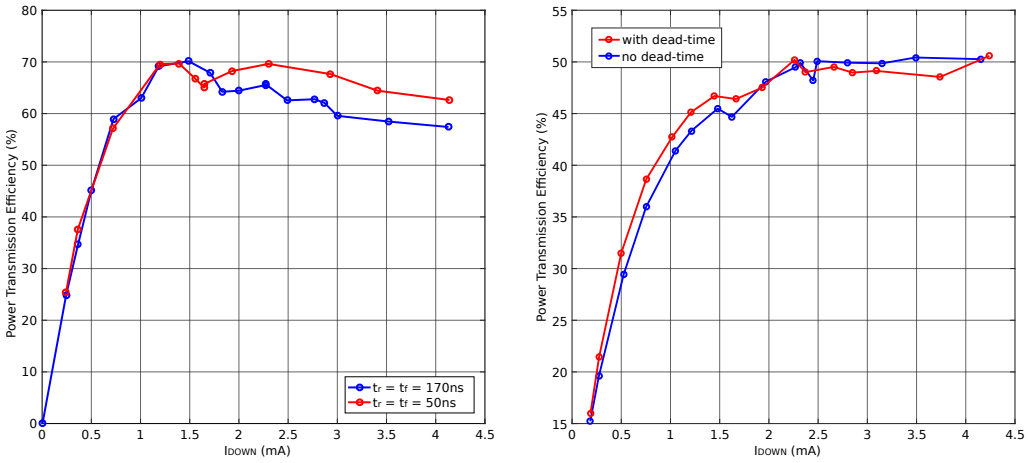
multimeters, a script written in MATLAB was used to calculate the PTE as follows:

$$V_{diff} = abs(V_{D1} - V_{D2}) \tag{6.2}$$

$$I_{DOWN} = abs(I_{cable} - mean(I_{cable})) \tag{6.3}$$

$$P_{chest} = mean(I_{DOWN} \times V_{diff}) \tag{6.4}$$

$$P_{brain} = I_{brain} \times V_{rect} \tag{6.5}$$



(a) Measured PTE using a function generator as the downlink driver with different transition times and with the uplink disconnected.

(b) Calculated PTE for PCU_v2 with and without a 25 ns dead-time.

Figure 6.11: Measured PTE with and without dead-time.

It is clear from Figure 6.11b that the achieved maximum PTE is less than the expected value by 17 %. This may be because during the experiment, the uplink connections were not removed from the PCU and the 4WIC board. Therefore, the coupled downlink signal on the uplink wires was dissipated by the termination resistance of the uplink; reducing the power delivered to the brain implant. It is also interesting to note that up to a load current of 2 mA, when a switch dead-time of 25 ns was applied, the PTE improved by approximately 1.5 %. As mentioned before, including a switch dead-time has reduced the peak current flowing through the cable; thereby increasing efficiency. Further tests are required to completely understand the various factors affecting the PTE, and also why it saturates at 50 % and not reaching the maximum value of 67 % as stated in [25].

6.2.2.5 Downlink Bit Error Rate

As with any communication system, it is important to ensure that the data is received and decoded correctly at all receiving ends of the system. Thus, the BER is a good performance measure, giving an indication of how many bits are decoded/received incorrectly. Due to time constraints, priority was given to the uplink system with regards to data recovery. However, simple tests such as, visual inspection of the data and clock recovered at the 4WIC were held, with the corresponding waveforms shown in Figure 6.12. Such tests were performed using a single brain implant, with a data rate of 100 kbps without any load on the rectifier's output.

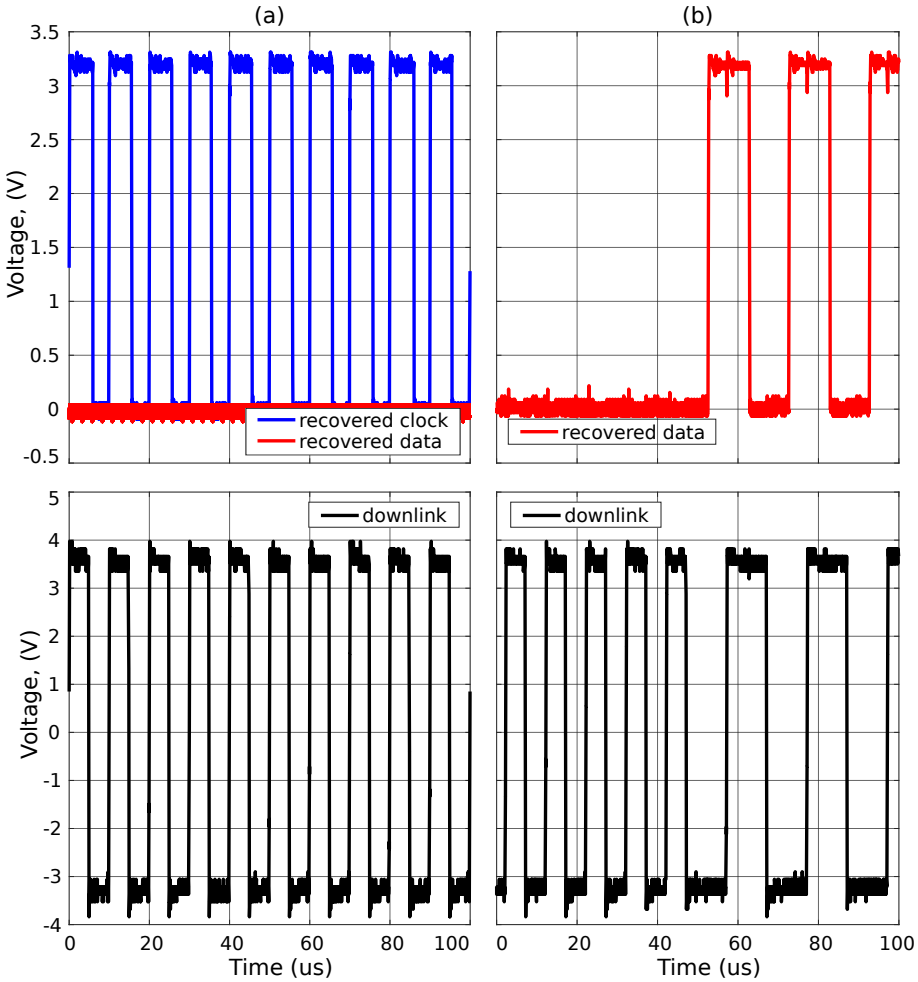


Figure 6.12: Measured results – 4WIC successfully recovers clock and data from differential downlink signal sent by the PCU; (a) 100 kHz signal on data results in a 100 kHz clock and a constant logic low for the data; (b) data looped from all 0s, to alternating - data recovered correctly.

6.2.3 Uplink

With several variables affecting the uplink interface, it proved to be quite a challenge to test the interface, and obtain consistent results. This primarily applies to the architecture using the tunable low pass filter, as it requires probing each output and ensuring that the desired change is being observed whilst tuning the circuitry. On the other hand, for the other architecture used, that is, a comparator with a tunable hysteresis, it has only one variable to tune, namely hysteresis. Before going into detail on the BER however, it is first worth confirming the theories presented earlier about the slew rate of the uplink drivers at the brain implant.

6.2.3.1 Slew Rate

The ideas mentioned earlier with regards to the slew rate were executed in an experiment to validate against the expected results. The plot in Figure 6.13 is the result of the bit sequence 1-0-0-0. The corresponding slew rates are: ■ 0.79 V/µs; ■ 0.91 V/µs; ■ 1.133 V/µs. These results concur with the theoretical expectations, such that the new 4-wire configuration has the highest slew rate amongst them all.

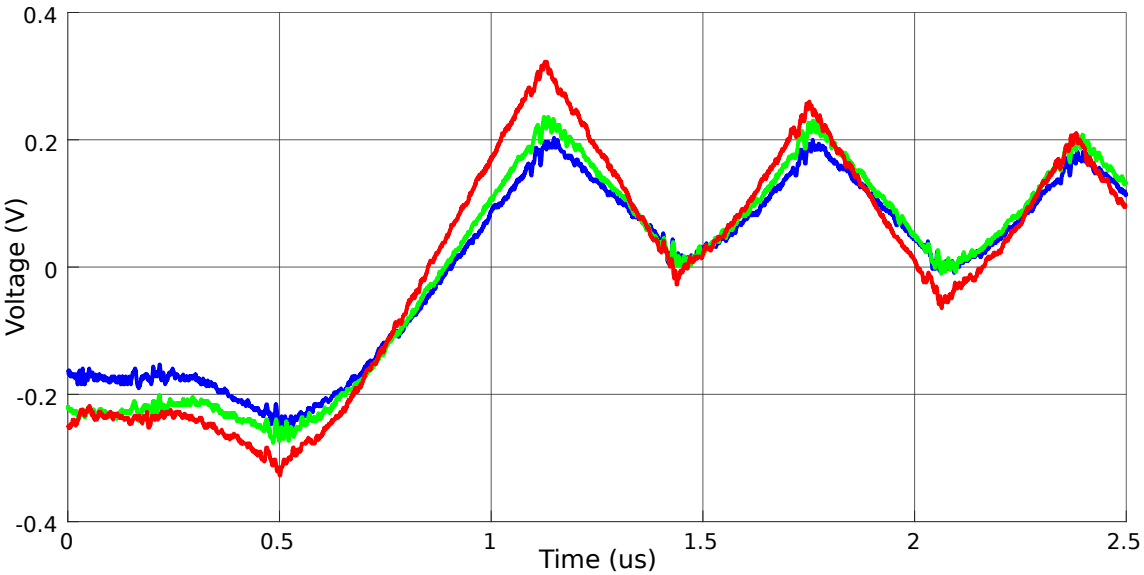


Figure 6.13: Different uplink slew rates according to configuration; ■ includes capacitance equalisation network; ■ excludes capacitance equalisation network; ■ without capacitance equalisation network and using the new 4-wire configuration.

6.2.3.2 Uplink Bit Error Rate

The BER was tested at two data rates, that is, 1.6 Mbps and 800 kbps. The 4WIC was connected to an isolator (ISO7320) to ensure an isolated ground. Additionally, to avoid loading the rectifier with the isolator's quiescent current, ISO7320's supply rails (for the 4WIC's side) were powered through an isolated power supply. On the other side, the isolator chip was powered using the 3.3 V supply available on the PCU. The uplink phase encoded signal and an enable signal were fed to the inputs of the isolator chip at the required frequencies by a function generator. Moreover, the configuration that resulted with the smallest slew rate (used in [25]) was used to ensure that the system works for the worst case scenario. However, from the uplink's point of view, this author suggests removing the capacitance equalisation network, applying the new wire configuration for the Cooper cable, and also using a termination resistance of approximately 300 Ω. Last but not least, this was tested by using the complex architecture incorporating a subtractor, a tunable LPF and a comparator, as this required most of the tuning (the termination resistor was set to 300 Ω). With respect to the comparator (with adjustable hysteresis), only a visual verification was carried out to check that the data was correct. The results for the former are found in Table 6.1.

Table 6.1: BER results for uplink at 1.6 Mbps and 800 kbps.

Data Rate	1.6 Mbps	800 kbps	800 kbps
Data Packet	2396745_{10}	2396745_{10}	2396745_{10}
Total number of packets sent	1,385,057	627,459	2,233,003
Amount of correct packets	1,385,050	627,444	2,215,161
Amount of wrong packets	7	15	17,842
% wrong packets	0.00051	0.00249	0.8
Operating Conditions	$V_{DOWN} = 6.5\,V$, $V_{optrode} = 5.17\,V$	$V_{DOWN} = 6.3\,V$, $V_{optrode} = 5\,V$	$V_{DOWN} = 6.3\,V$, $V_{optrode} = 4.98\,V$

All tests were performed using architecture (c) in Figure 4.14.
One packet is 26 bits long, 2 of which are synchronisation bits (1-0).

It is important to point out that in all instances, no wrong data was received at the GUI. This means that all errors were identified before being sent to the GUI. However, it

may also be the case that some packets were missed due to certain bits not being within the set pulse width thresholds. Due to a very small number of packets not being decoded correctly, further testing is required to analyse why these packets are not being received. This is something that takes a lot of time since the baud rate of the UART is quite low. Therefore, for the UART interface to keep up, the uplink data rate needs to be decreased considerably – to a rate of 200 packets per second. Thus, to obtain at least a million packets, it takes at least three hours to complete.

Similar tests were performed for the second architecture consisting of a comparator with adaptive hysteresis. This solution showed promising results, especially due to its small volume. Additionally, its hysteresis can easily be made to change using the FPGA, by altering the current multi-turn potentiometer design into a digital potentiometer of an appropriate size. Further testing however, needs to be done to check whether this solution consumes more power than the other architecture.

6.3 Summary

This chapter first presents the testing setups used to characterise the implemented system. This is then followed by the results obtained for each module with a discussion as to whether such results are expected, and why. All results are summarised in Table 6.2.

Table 6.2: Testing, Results and Discussion - summary table

Function	Parameter	Value
Power in - to PCU	AV_{DD}, DV_{DD}	5 V, 3.3 V
Power out - to PMs	$V_{DOWN,min}$, $V_{DOWN,max}$, $I_{DOWN,max}$, $Efficiency_{max}$	5.5 V, 11 V, 22 mA, 86 %
Current Feedback	F_S, Resolution, $t_{s,max}$	100 kSps, 8 bits, 1.5 ms
Downlink Driver	$t_{r,max}$, $t_{f,max}$, Data rate, PTE_{max}	250 ns, 80 ns, 100 kbps, 50 %
Uplink Receiver	DV_{DD}, $Data\ rate_{max}$, BER_{max}, $Slew\ Rate_{max}$	3.3 V, 1.6 Mbps, 0.8 %, 1.13 V/µs

Chapter 7

Conclusion

THIS thesis has addressed the design and implementation requirements of a PCB based chest device, focusing on the interface between this device and other peripheral modules.

The initial analysis of the contemporary literature reveals that as the complexity of implantable systems increases, new types of such systems are emerging comprising of multi-module systems. Since such systems are generally composed of one master and multiple slave devices, they require an interface for power delivery and data communication. The CANDO system, which this work forms part of, uses a master chest unit and multiple peripheral implants (in the brain); aiming at providing a closed-loop therapy for focal epilepsy.

Thus, this work focuses on the master chest unit, and any electronics required to interface with the peripheral implants. The AC-coupled interface makes use of 4-wires for power delivery and full-duplex data communication. Square waves are used to deliver both power and phase encoded data from the chest unit at a bit rate of 100 kbps. Data communication in the other direction uses phase encoding with a maximum bit rate of 1.6 Mbps.

A novel adaptive power delivery method with full duplex data communication was used in this work. The proposed power management system can deliver up to 120 mW of power at 6 V (to the peripheral implant) superimposed on a phase encoded serial bit

stream with a data rate of 100 kbps (downlink). The maximum efficiency achieved for this implementation is 86%, with the dynamic power dissipation of the drivers being the dominant source of power loss across all load current ranges. This loss can however be reduced by introducing a dead-time in the driver. Measured results show that a worst case recovery for a 6 V constant supply at the peripheral implant takes 1.5 ms for a step of 22 mA.

Uplink communication is achieved through a separate pair of wires using phase encoding at a maximum data rate of 1.6 Mbps. Two architectures were implemented; with the design being configurable, depending on the characteristics of the waveform. Two prototype systems comprising of all the circuitry for the chest implant have been implemented, occupying 5×5 cm and 10×10 cm respectively, on a PCB substrate.

7.1 Publication Arising from this Work

A publication arising from this work is a paper entitled *Adaptive Power Regulation and Data Delivery for Multi-Module Implants*. This has been accepted for the IEEE Biomedical Circuits and Systems (BioCAS) Conference 2017. I co-authored this paper together with Dorian Haci, Sara S. Ghoreishizadeh, Yan Liu and Timothy G. Constandinou. A copy of the submitted paper is included in Appendix A.

7.2 Future Work

The end product of this project currently implements a configurable PCU whose parameters depend on the characteristics of the implantable cable and the optrodes. Further work and testing is required to obtain the optimal solution, especially in terms of area and efficiency, and to explore the advantages and disadvantages of this implementation.

Although the implementation for the current feedback system works, further investigation of the switch on-state resistance in relation to the current flowing through it and its supply voltage if required. This would increase the accuracy of the loop, ensuring that the right V_{DOWN} is set. At the expense of decreased efficiency, it may be feasible to

completely re-design the current feedback system, making use of a current sensing resistor instead. This resistor can either be a passive component, or the PCB/ASIC tracks may be used to obtain this resistance.

A further improvement could be that of integrating the whole chest unit, combining the FPGA board and the PCU into a single small PCB. This however, requires all parameters to be fixed so as to reduce the amount of pin headers required (and therefore area); permitting the design to be scaled down. Such an approach, applies also to the firmware used in the FPGA; when parameters are fixed, the algorithms can be optimised and the utilisation of resources reduced. A point not to be overlooked is the track lengths of the switches. Whereas currently PCU_v2 has the track lengths matched, those on the FPGA board are not. Integrating both PCBs into one ensures that switch edges arrive exactly at the same time at the switch inputs.

Although switch dead-time and its effect on efficiency has been discussed, and its effect on efficiency, and the current waveform investigated, further work is required to identify the effect of longer dead-times. Given that the downlink driver's efficiency is expected to rise, one may ask whether the PTE will increase as well. Another question posed relates to at what value (t_d) does the effect of switch dead-time on downlink driver efficiency becomes negligible, or worse, have negative effects on the optrode voltage.

Additional optimisations for the uplink interface are necessary in order to reduce the bandwidth of the signal and the interference from the downlink as well. Apart from the improvements mentioned in the course of this thesis, it may also be worth investigating Multi-Level Transmit (MLT)-3 encoding on the phase encoded data signal. This can be done by using the current 4WIC as it offers three states, namely *high*, *low*, and *high impedance*. Ideally, however, three different voltages are used instead.

Further testing on the board is required, to examine the effect of using DC/DC converters in relation to the Electromagnetic Interference (EMI) generated by these devices. The device used in this work uses a switching frequency of 1 MHz. Even though this is high (compared to the audible range), during burst-mode operation the resulting switching frequency can be less; possibly occupying the audible frequency range during

lighter loads.

The system presented in this work has been tested with only one 4WIC. This however, will be used with up to 16 devices connected in parallel to the implantable cable. Therefore, the system needs to be tested with multiple devices to observe its dynamic behaviour whilst operating with multiple optrodes with a varying load.

Last but not least, possibly in the near future, the architecture used in this work can be applied to multiple clusters of PMs (a cluster has multiple PMs all connected in parallel to a common cable). Hence, a multiple channel solution would be required, especially in the instance where a cluster contains identical PMs, but the PMs are different from one cluster to another.

Bibliography

[1] S. Bhunia, S. Majerus, and M. Sawan, *Implantable Biomedical Microsystems: Design Principles and Applications*. Elsevier, Jan. 2015.

[2] C. W. Moss and P. H. Peckham, "Neural prosthesis system and method of control," U.S. Patent US20 170 100 587 A1, Apr., 2017.

[3] MEDEL, "Cochlear Implants for Hearing Loss." [Online]. Available: http://www.medel.com/

[4] R. L. Hart, N. Bhadra, F. W. Montague, K. L. Kilgore, and P. H. Peckham, "Design and Testing of an Advanced Implantable Neuroprosthesis With Myoelectric Control," *IEEE Transactions on Neural Systems and Rehabilitation Engineering*, vol. 19, no. 1, pp. 45–53, Feb. 2011.

[5] B. Smith, T. J. Crish, J. R. Buckett, K. L. Kilgore, and P. H. Peckham, "Development of an implantable networked neuroprosthesis," in *Conference Proceedings. 2nd International IEEE EMBS Conference on Neural Engineering, 2005.*, Mar. 2005, pp. 454–457.

[6] M. Arent, "Network for implanted computer devices," U.S. Patent US6 358 202 B1.

[7] K. L. Kilgore, P. H. Peckham, T. J. Crish, and B. Smith, "Neural prosthesis," U.S. Patent US9 108 060 B2, Aug., 2015.

[8] Cleveland FES Center, "Networked Neuroprosthetic (NNP) System." [Online]. Available: http://fescenter.org/research/technology-programs/networked-neuroprosthetic-system-nnps/

[9] H. Zhao, F. Dehkhoda, R. Ramezani, D. Sokolov, P. Degenaar, Y. Liu, and T. Constandinou, "A CMOS-based neural implantable optrode for optogenetic stimulation and electrical recording," in *2015 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct. 2015, pp. 1–4.

[10] Q. Fang, S. Y. Lee, H. Permana, K. Ghorbani, and I. Cosic, "Developing a Wireless Implantable Body Sensor Network in MICS Band," *IEEE Transactions on Information Technology in Biomedicine*, vol. 15, no. 4, pp. 567–576, Jul. 2011.

[11] P. R. Troyk and N. d. N. Donaldson, "Implantable FES Stimulation Systems: What is Needed?" *Neuromodulation: Journal of the International Neuromodulation Society*, vol. 4, no. 4, pp. 196–204, Oct. 2001.

[12] N. L. Opie, A. N. Burkitt, H. Meffin, and D. B. Grayden, "Heating of the Eye by a Retinal Prosthesis: Modeling, Cadaver and In Vivo Study," *IEEE Transactions on Biomedical Engineering*, vol. 59, no. 2, pp. 339–345, Feb. 2012.

[13] V. Giagka, C. Eder, N. Donaldson, and A. Demosthenous, "An Implantable Versatile Electrode-Driving ASIC for Chronic Epidural Stimulation in Rats," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 3, pp. 387–400, Jun. 2015.

[14] L. H. Jung, N. Shany, A. Emperle, T. Lehmann, P. Byrnes-Preston, N. H. Lovell, and G. J. Suaning, "Design of Safe Two-Wire Interface-Driven Chip-Scale Neurostimulator for Visual Prosthesis," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 9, pp. 2217–2229, Sep. 2013.

[15] S. S. Ghoreishizadeh, D. Haci, Y. Liu, and T. G. Constandinou, "A 4-wire interface SoC for shared multi-implant power transfer and full-duplex communication," in *2017 IEEE 8th Latin American Symposium on Circuits Systems (LASCAS)*, Feb. 2017, pp. 1–4.

[16] N. Tran, S. Bai, J. Yang, H. Chun, O. Kavehei, Y. Yang, V. Muktamath, D. Ng, H. Meffin, M. Halpern, and E. Skafidas, "A Complete 256-Electrode Retinal Prosthesis Chip," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 751–765, Mar. 2014.

[17] S. Banzi, E. Mainardi, and A. Davalli, "A CAN-based distributed control system for upper limb myoelectric prosthesis," in *2005 ICSC Congress on Computational Intelligence Methods and Applications*, 2005, pp. 6 pp.–.

[18] R. Ramezani, F. Dehkhoda, A. Soltan, P. Degenaar, Y. Liu, and T. Constandinou, "An optrode with built-in self-diagnostic and fracture sensor for cortical brain stimulation," in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct. 2016, pp. 392–395.

[19] P. E. K. Donaldson, "The Cooper cable: an implantable multiconductor cable for neurological prostheses," *Medical and Biological Engineering and Computing*, vol. 21, no. 3, pp. 371–374, May 1983. [Online]. Available: https://link.springer.com/article/10.1007/BF02478508

[20] Microsemi, "IGLOO nano Starter Kit." [Online]. Available: https://www.microsemi.com/products/fpga-soc/design-resources/dev-kits/igloo/igloo-nano-starter-kit

[21] Maxim Integrated, "MAX4679 Datasheet." [Online]. Available: https://www.maximintegrated.com/en/products/analog/analog-switches-multiplexers/MAX4679.html

[22] T. Regan, J. Munson, G. Zimmer, and M. Stokowski, "Current Sense Circuit Collection."

[23] B. McGovern, R. B. Palmini, N. Grossman, E. M. Drakakis, V. Poher, M. A. A. Neil, and P. Degenaar, "A New Individually Addressable Micro-LED Array for Photogenetic Neural Stimulation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 4, no. 6, pp. 469–476, Dec. 2010.

[24] Linear Technology, "LTC3130 Datasheet." [Online]. Available: http://www.linear.com/product/LTC3130

[25] S. S. Ghoreishizadeh, D. Haci, Y. Liu, N. Donaldson, and T. G. Constandinou, "Four-Wire Interface ASIC for a Multi-Implant Link," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. PP, no. 99, pp. 1–12, 2017.

[26] F. Taylor and A. Williams, *Electronic Filter Design Handbook, Fourth Edition*, 4th ed. McGraw-Hill Education, Jul. 2006.

[27] A. Mifsud, "Direct Digital Synthesis Radio Frequency Arbitrary Function Generator using an FPGA," Bachelor dissertation, University of Malta, Malta.

Appendix A

Publication arising from this work

Adaptive Power Regulation and Data Delivery for Multi-Module Implants

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***Abstract*—Emerging applications for implantable devices are requiring multi-unit systems with intrabody transmission of power and data through wireline interfaces. This paper proposes a novel method for power delivery within such a configuration that makes use of closed loop dynamic regulation. This is implemented for an implantable application requiring a single master and multiple identical slave devices utilising a parallel-connected 4-wire interface. The power regulation is achieved within the master unit through closed loop monitoring of the current consumption to the wired link. Simultaneous power transfer and full-duplex data communication is achieved by superimposing the power carrier and downlink data over two wires and uplink data over a second pair of wires. Measured results using a fully isolated (AC coupled) 4-wire lead, demonstrate this implementation can transmit up to 120 mW of power at 6 V (at the slave device, after eliminating any losses). The master device has a maximum efficiency of 80 % including a dominant dynamic power loss. A 6 V constant supply at the slave device is recovered 1.5 ms after a step of 22 mA.**

I. Introduction

Implantable Medical Devices (IMDs) such as pacemakers, cochlear implants and deep brain stimulators have already demonstrated a significant impact to the quality of life of millions of users. These devices interface with the human body by monitoring and/or manipulating activity, and are able to restore function by bypassing dysfunctional organs/pathways. Although the field of IMDs is not new (the first implantable pacemaker dates back to 1959), with the advent of microtechnology and capability this brings, the ambition and reach of such devices are now targeting significantly more advanced disease/treatments. Examples include neural prostheses for depression, eating disorders and epilepsy [1].

Recently, due to improved power efficiency and integration density, the volume per implant and power required per single function have been significantly reduced. We are now seeing new opportunities emerging for closed-loop therapies both in academia and industry. Although the power per given function is generally decreasing, the complexity of the overall systems is increasing (for example including more channels, more capability), and thus the power budget remains a challenge [2]. The limitations imposed by the energy density of implantable batteries, and safe operating conditions for thermal dissipation present challenging trade-offs.

An emerging approach to mitigating such challenges is to employ multi-module, or multi-node implants as illustrated in Fig. 1. By effectively partitioning the system into physically-separated units, with the different functions located at different sites. The most common configuration is to have one relatively large central implant (CI), typically implanted in the upper chest that houses the battery, processing and communication functions. Smaller peripheral implant (PI) units can then be located close to the target interface sites. One good example is the Networked Neuroprosthesis System (NNP) developed at Case Western Reserve University [3]. This allows for a single CI unit to be connected to multiple PI units via a digital wireline interface. As this however is targeted to Functional Electrical Stimulation (FES) applications, the required number of stimulation and/or recording channels (and bandwidth) is limited.

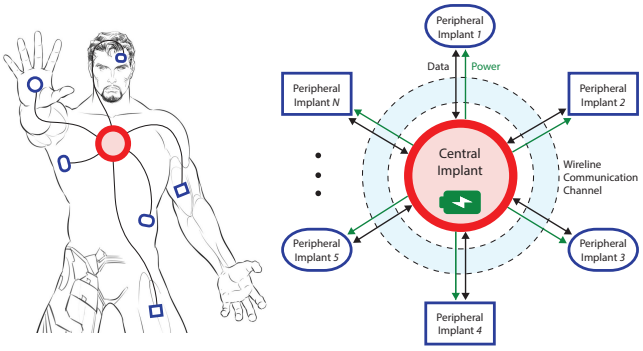

Fig. 1. Concept of wired intrabody multi-module Implants.

The work presented in this paper has been developed as part of the CANDO project (www.cando.ac.uk). CANDO aims to develop an implantable device to provide a closed-loop therapy for focal epilepsy. The CANDO system consists of one CI unit for control and power and multiple PI units for bidirectional neural interfacing [4], [5]. The different units are connected via a shared implantable lead.

This paper describes a new method developed to transmit and adaptively regulate power (whilst also communicate data) from a single CI to multiple PIs through a wired communication channel. The rest of this paper is organised as follows: Section II describes the dynamic power regulation concept; Section III describes the system architecture and circuit implementation; Section IV presents measured results; and Section V concludes the work.

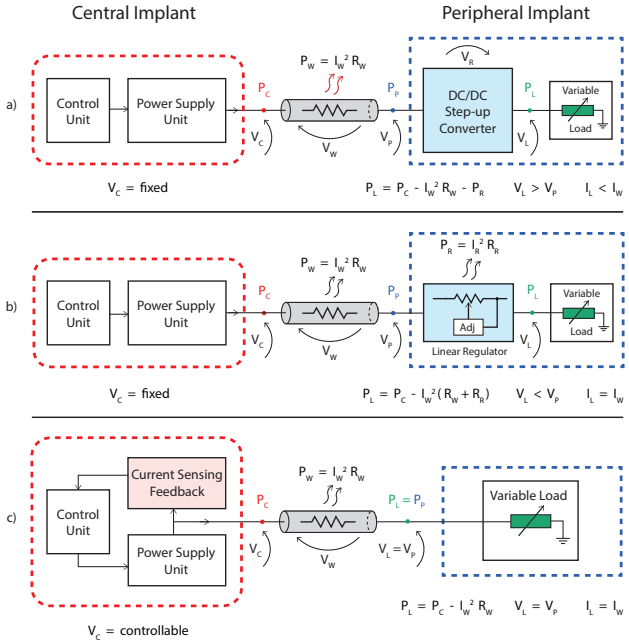

Fig. 2. Three methods for power delivery, utilising: (a) DC/DC conversion; (b) linear regulation; (c) adaptive, closed-loop regulation.

II. Intrabody Power Transmission

The need to reliably transmit power from a single CI to multiple PI modules poses certain challenges. It is essential that any configuration adopted is safe, reliable and efficient. For these reasons the majority of such links are wire-based despite there being significant effort in the community to develop various wireless modalities. Even so, wireline transmission poses certain challenges – the number of wires must be kept to a minimum, DC voltages must be avoided, and there is a need to achieve full duplex communication.

For the system to operate reliably, any transmission scheme must guarantee uninterrupted power delivery with a constant supply (V_L) irrespective of battery level, a load that changes with configuration, and a dynamic current profile.

Different methods for delivering dynamic power through an implanted cable have been reported in the literature [6] [7]. The power regulation typically occurs within the PI units, employing either DC/DC converters and/or linear voltage regulators. For systems using DC/DC converters (Fig. 2(a)) it is possible to generate boosted supply voltages, albeit sacrificing current supply and increasing complexity (silicon area and/or off-chip discrete components). Using linear regulators on the other hand provide a simple, compact solution at the expense of efficiency. Furthermore, it is essential to provide a significantly higher voltage level to compensate for the regulator drop (Fig. 2(b)). Both methods require additional circuitry at the PI module, increasing power and adding to the inevitable IR loss on the wires of the communication channel.

The method proposed herein mitigates the need to coarse regulation within the PI modules, by instead adaptively regulating the power within the CI unit through closed-loop feedback. By continually sensing the current supply (I_W) within the CI, the IR drop across the cable can be calculated (Fig. 2(c)). The CI output voltage V_C can subsequently be dynamically adjusted based on the instantaneous load V_C to ensure a constant voltage level is received at the PI modules. As a result, the power loss in the delivery process is due exclusively to the IR drop across the wired link.

This can be extended to multiple identical PI modules – in this case the current measured by the feedback path corresponds to the sum of the load currents of all the PIs, with the voltage received being common to all units.

III. System Implementation

As mentioned previously, the key requirements for the system implemented are safety, reliability and efficiency. To reduce the risk of corrosion due to DC electric fields, in addition to a failsafe in the event of a conductor breakage, DC blocking capacitors are used. The system implemented uses an implantable lead with 4-wires organised as two differential wire pairs: one for power and downlink data transmission (CI to PIs), and the other for uplink data transmission (PIs to CI). The interface is AC-coupled using phase (Manchester) encoding for data. In our application, the CI unit needs to deliver a maximum current of 20 mA at 6 V to all the PI modules. The communication link is a lossy cable with a total resistance for a pair of wires of 220 Ω (adapted from [8]). PI to CI data communication is to have a maximum data rate of 1.6 Mbps, and 100 kbps vice versa. More details on the interface can be found in [8], [9].

The system presented herein has been implemented on a PCB to interface between an FPGA-based controller and the 4-wire implantable lead. It receives commands and data packets through a UART connection from a PC-based GUI and updates the downlink and uplink modules as necessary. The top level architecture of this system is divided into five main blocks: (1) power management; (2) downlink drivers; (3) feedback; (4) uplink receivers; and (5) digital controller. The circuit implementation of the 4-wire PCB interface is shown in Fig. 3.

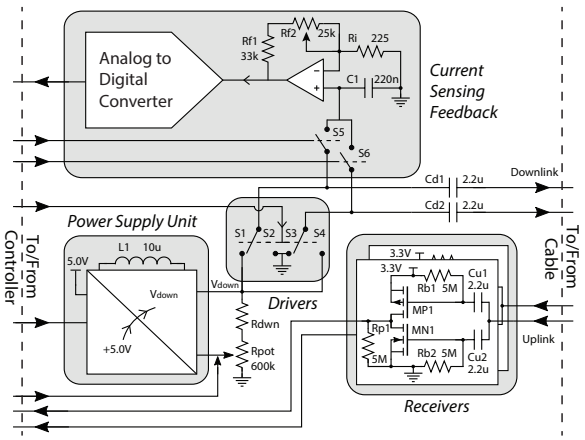

Fig. 3. Top level circuit schematic for the power management and data transceiver within the CI unit.

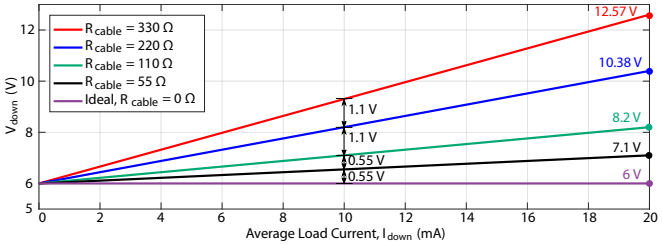

Fig. 4. V_{down} vs. I_{down} for different values of R_{cable}.

A. Power Management

The voltage, V_{down}, required to maintain a constant 6 V supply to the PI modules, depends on the current flowing through the communication link. This is described in Eqn 1.

$$V_{down} = 6\,V + I_{down}R_{cable} \tag{1}$$

Considering different values for R_{cable} gives the characteristics shown in Fig. 4. These show that the choice of cable is critical since this directly affects power losses in the communication link and thus the efficiency of the whole system. For an R_{cable} of 220 Ω, a DC-DC converter was chosen (LTC3130) so as to be able to supply a voltage (at the CI unit side) of between 6 and 10.5 V from a 5 V supply. The output voltage of this boost converter is set by a potential divider connected to the output pin (V_{down}), feedback pin, and ground. In our system, this is provided through digital potentiometers that are controlled by the FPGA. Three 200 $k\Omega$, 32-tap, digital potentiometers are here connected in series, ensuring a high resistance so as to minimise power consumption.

B. Downlink Drivers

This was implemented by using four SPST (2 NO, 2 NC) switches, S1 to S4 (available in one package as the MAX4679), connected as one SPDT switch per pair (1 NO, 1 NC) with inverted input connections (V_{down} and GND). Alternating between V_{down} and GND, these switches deliver power and Manchester encoded data (at 100 kbps) concurrently through the cable. To reduce the power losses at the chest unit it is important to have switches with a very low on-resistance. Also break-before-make circuitry is essential, to ensure that the normally closed switch is disconnected before connecting the normally open switch (and vice-versa). This is required to avoid an instantaneous short circuit at the transitions (i.e. between V_{down} and GND).

C. Current Sensing Feedback

To be able to adjust V_{down} depending on the load current, a current sense circuit is required. This is usually achieved by measuring a voltage drop across a current sense resistor placed in series with the load which results in an additional loss of power. In this case, however, the voltage drop across the on-resistance of the switches was measured instead. To avoid dealing with high voltages, low side current sensing was implemented. This required two SPST switches (S5 and S6) so as to multiplex the driver output that is connected to ground. The switch outputs are then sampled by a hold capacitor, and an amplifier to make use of the full scale input range of the ADC. The value for the hold capacitor was set so as to reduce the voltage droop from leakage currents, limit the change in voltage from charge injection, and to ensure that the capacitor charges to the set voltages within the available minimum time.

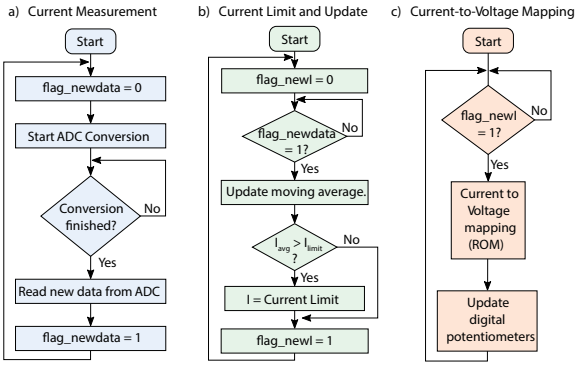

Fig. 5. Digital control algorithms for evaluation and feedback (implemented as a finite state machine on FPGA).

D. Uplink Receivers

For the uplink receiver, a CMOS inverter is used for each wire so as to be able to monitor each line separately. The gate of each MOSFET is biased at either 3.3 V or ground to make sure that both MN_x and MP_x are off during idle operation (i.e. no activity on uplink). Thus for a valid output value during idle operation (as both transistors are off), a pull-down high-value resistor is connected to the output of the inverter. During normal operation, the received uplink signal is superimposed on the DC gate voltage by a capacitor. The inverter then converts this signal to an LVCMOS33 digital signal which is then processed by the FPGA to decode the data received.

E. Digital Controller

This was implemented in VHDL on an IGLOO Nano FPGA board (AGL250V2-VQG100 Starter Kit) consisting of several modules to control and monitor each part of the system based on the commands received through UART. During normal operation, voltage regulation is achieved by first requesting a new acquisition from the ADC to sample the current flowing

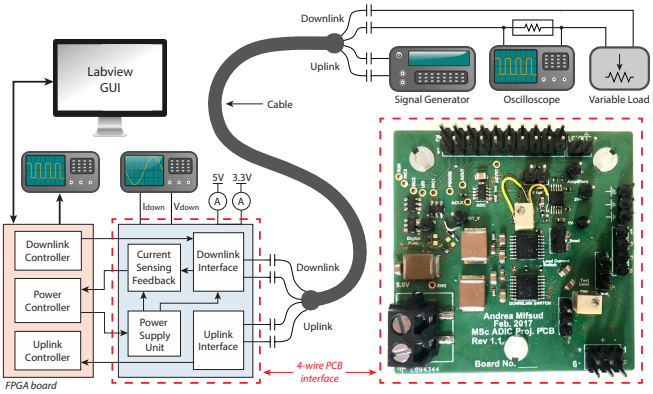

Fig. 6. Experimental setup and prototype 4-wire interface board within CI.

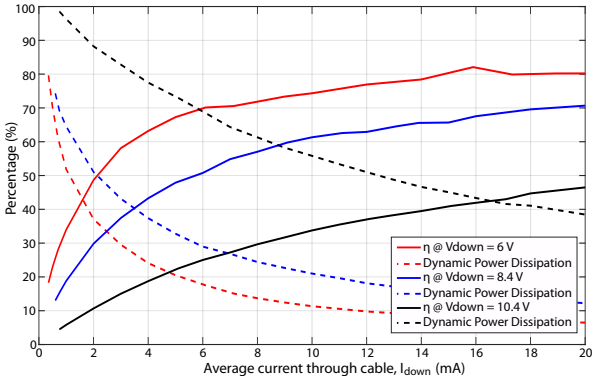

Fig. 7. System efficiency for different values of V_{down}, and load current.

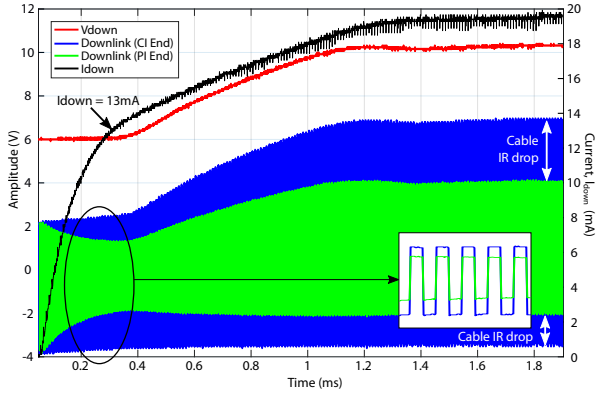

Fig. 8. System step response. $I_{dwn} = 22\,mA$ at $V_{down} = 10.4\,V$, $R_L = 470\,\Omega$

through the cable. Once the new sample is received, an 8-sample moving average is updated, and the result mapped to a voltage by a ROM which stores this mapping based on specific parameters of the system (see Fig. 5). This voltage is then converted into a number of taps, for the digital potentiometers to be updated, thus updating V_{down}. For data communication, data is sent to the PIs by controlling the drivers as required, and any new data received from the PIs is sent through UART. During idle operation, the downlink drivers are switched at a frequency of 100 kHz to keep transmitting power, whilst sending a logic low.

IV. Measured Results

The CI power delivery and downlink data communication was tested for various load conditions and V_{down} values using a dummy resistive load [8], as shown in Fig. 6. Two tests were carried out, one to determine the efficiency of the PCB based chest unit, and another for the worst case step-response of the system. Key system specifications are summarised in Table I.

TABLE I
Achieved System Specifications

Function	Parameters	Value
Power	V_{in}, $I_{down,max}$ $V_{down,min}$, $V_{down,max}$	5 V, 20 mA 5.5 V, 10.4 V
Feedback	F_s, Resolution, $t_{s,max}$	100 ksps, 8 bits, 1.5 ms
Driver	AVDD, DVDD t_r, t_f, Datarate	5.5-10.4 V, 3.3 V 250 ns, 100 ns, 100 kbps
Receiver	DVDD, $Datarate_{max}$	3.3 V, 1.6 Mbps

The measured results for efficiency are shown in Fig. 7. This shows that the efficiency increases when V_{down} decreases and(/or) when the load current, I_{down} increases. The main loss in the system is found to be dynamic power dissipation of the downlink drivers, measured at 8.6 mW for V_{down} of 6 V, and increasing by an order of magnitude at 10.4 V.

The stability of the system was tested by applying a step in I_{down} of 22 mA as illustrated in Fig. 8. Initially, the current settles at approximately 13 mA, increasing linearly as V_{down} increases to compensate for the voltage drop on the cable, until the current measurement saturates at 20 mA. Thus, the measured worst case settling time of the system is 1.5 ms.

V. Conclusion

This paper has presented a novel adaptive power delivery method with full duplex data communication for a wired multi-module implantable device. A prototype system testing the circuit implementation of the central implant has been implemented occupying 5×5 cm on a PCB substrate. The proposed power management system can however, deliver up to 120 mW power at 6 V (to the peripheral implant) superimposed on a phase encoded serial bitstream with datarate of 100 kbps (downlink). The maximum efficiency achieved for this implementation is 80%, with the dynamic power dissipation of the drivers being the dominant source of power loss across all load current ranges. Measured results show that a worst case recovery for a 6 V constant supply at the peripheral implant takes 1.5 ms for a step of 22 mA. Uplink communication is achieved through a separate pair of wires using phase encoding at a maximum datarate of 1.6 Mbps.

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References

[1] S. Bhunia *et al.*, *Implantable Biomedical Microsystems: Design Principles and Applications*. Elsevier, 2015.
[2] T. Lehmann *et al.*, "Low-power circuit structures for chip-scale stimulating implants," in *Proc. IEEE APCCAS*, 2012, pp. 312–315.
[3] B. Smith *et al.*, "Development of an implantable networked neuroprosthesis," in *Proc. IEEE/EMBS Neural Engineering*, 2005, pp. 454–457.
[4] H. Zhao *et al.*, "A CMOS-based neural implantable optrode for optogenetic stimulation and electrical recording," in *Proc. IEEE BioCAS Conference*, 2015, pp. 1–4.
[5] R. Ramezani *et al.*, "An optrode with built-in self-diagnostic and fracture sensor for cortical brain stimulation," in *Proc. IEEE BioCAS Conference*. IEEE, 2016, pp. 392–395.
[6] L. H. Jung *et al.*, "Towards a chip scale neurostimulator: System architecture of a current-driven 98 channel neurostimulator via a two-wire interface," in *IEEE EMBS Conference*, 2011.
[7] N. Tran *et al.*, "A complete 256-electrode retinal prosthesis chip," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 3, pp. 751–765, 2014.
[8] S. S. Ghoreishizadeh *et al.*, "Four-wire interface ASIC for a multi-implant link," *IEEE Transactions on Circuits and Systems I*, pp. 1–12, 2017.
[9] S. S. Ghoreishizadeh *et al.*, "A 4-wire interface SoC for shared multi-implant power transfer and full-duplex communication," in *Proc. IEEE LASCAS*, 2017.